(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号
特開2003－204243
（P2003－204243A）
(43)公開日　平成15年７月18日(2003.7.18)

(51)Int.Cl.[7]	識別記号	ＦＩ		テーマコード*（参考）
Ｈ０３Ｈ　9/25		Ｈ０３Ｈ　9/25	Ａ	５Ｊ０９７
			Ｃ	
9/145		9/145	Ａ	
			Ｃ	
			Ｚ	

審査請求　未請求　請求項の数28　ＯＬ　（全 18 頁）

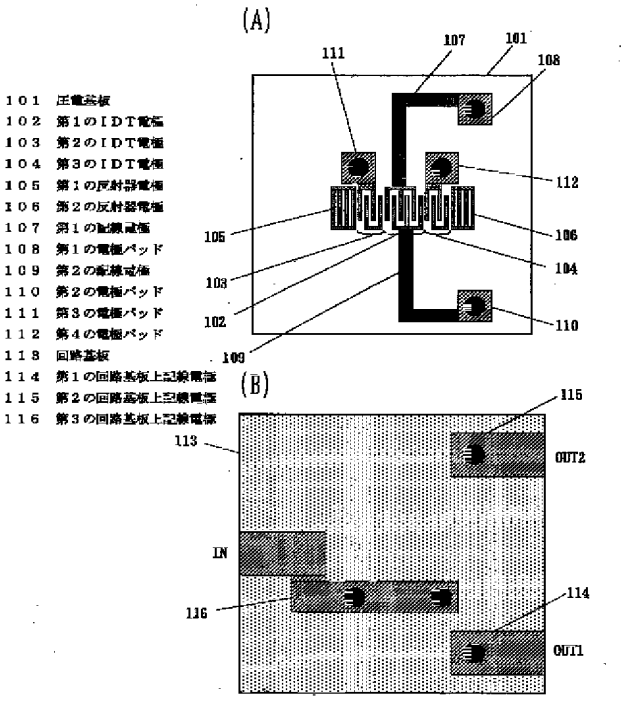
(21)出願番号　特願2002－311730(P2002－311730)
(22)出願日　平成14年10月25日(2002.10.25)
(31)優先権主張番号　特願2001－330435(P2001－330435)
(32)優先日　平成13年10月29日(2001.10.29)
(33)優先権主張国　日本（ＪＰ）

(71)出願人　000005821
松下電器産業株式会社
大阪府門真市大字門真1006番地
(72)発明者　中村　弘幸
大阪府門真市大字門真1006番地　松下電器産業株式会社内
(72)発明者　大西　慶治
大阪府門真市大字門真1006番地　松下電器産業株式会社内
(74)代理人　100092794
弁理士　松田　正道

最終頁に続く

(54)【発明の名称】　弾性表面波フィルタ素子、弾性表面波フィルタ、及びそれを用いた通信機器

(57)【要約】
【課題】　平衡型端子を有する弾性表面葉フィルタに関して、バランス特性が劣化するという課題があった。
【解決手段】　第１のＩＤＴ電極１０２の一方の電極指は第１の配線電極１０７を介して第１の電極パッド１０８に接続される。第１のＩＤＴ電極１０２の他方の電極指は第２の配線電極１０９を介して第２の電極パッド１１０に接続される。第２、第３のＩＤＴ電極１０３、１０４の一方の側の電極指は実質上直接に第３、第４の電極パッド１１１、１１２に接続される。



【特許請求の範囲】
【請求項１】　圧電基板と、
前記圧電基板上に形成された複数のインターディジタルトランスデューサ電極（ＩＤＴ電極）とを備えた弾性表面波フィルタ素子であって、
前記複数のＩＤＴ電極の内、少なくとも一つのＩＤＴ電極は平衡型端子に接続され、他のＩＤＴ電極は平衡型端子または不平衡型端子に接続され、
前記少なくとも一つのＩＤＴ電極に接続されるべき又は接続された第１の配線電極手段と、前記他のＩＤＴ電極に接続されるべき又は接続された第２の配線電極手段とが、互いに異なる平面上に配置されている弾性表面波フィルタ素子。
【請求項２】　前記第１及び第２の配線電極手段の内、一方の前記配線電極手段が前記圧電基板の主面上に配置されており、他の前記配線電極手段は前記圧電基板が実装されるべき回路基板上に配置されている請求項１に記載の弾性表面波フィルタ素子。
【請求項３】　（１）前記第１及び第２の配線電極手段の内、一方の前記配線電極手段が前記圧電基板上に形成されており、且つ、他方の前記配線電極手段は前記圧電基板が実装されるべき回路基板の内層電極である、又は、（２）前記第１及び第２の配線電極手段の内、一方の前記配線電極手段は前記圧電基板が実装されるべき回路基板上に形成され、且つ、他方の前記配線電極手段は前記回路基板の内層電極である請求項１に記載の弾性表面波フィルタ素子。
【請求項４】　前記第１及び第２の配線電極手段の内、一方の前記配線電極手段が圧電基板の主面上に設けられており、他方の前記配線電極手段が前記圧電基板の前記主面上に形成された保護膜上に設けられている請求項１に記載の弾性表面波フィルタ素子。
【請求項５】　前記保護膜が誘電体薄膜である請求項４に記載の弾性表面波フィルタ素子。
【請求項６】　前記弾性表面波フィルタ素子が、第１、第２、第３のＩＤＴ電極と少なくとも２つの反射器電極とを弾性表面波の伝搬方向に沿って配置した縦モード型の弾性表面波フィルタ素子であって、
前記第１のＩＤＴ電極の両側に前記第２、第３のＩＤＴ電極が配置される構成である請求項１に記載の弾性表面波フィルタ素子。
【請求項７】　前記圧電基板上に設けられた第１及び第２の電極パッドと、
前記圧電基板上に設けられた、前記第２のＩＤＴ電極に実質上直接に接続された第３の電極パッドと、
前記圧電基板上に設けられた、前記第３のＩＤＴ電極に実質上直接に接続された第４の電極パッドとを備え、
（１）前記第１の配線電極手段手段は、一対の配線電極として前記圧電基板上に設けられており、且つ、（２）前記第１のＩＤＴ電極は、平衡型であって、しかも前記一対の配線電極の各配線電極を介して前記第１、第２の電極パッドに接続されており、
前記第２の配線電極手段は、前記回路基板に設けられており、
前記弾性表面波フィルタ素子が、前記回路基板に実装されることにより、前記第３、第４の電極パッドが、前記第２の配線電極手段に接続される請求項６に記載の弾性表面波フィルタ素子。
【請求項８】　前記圧電基板上に設けられた、前記第１のＩＤＴ電極に実質上直接に接続された第１及び第２の電極パッドと、
前記圧電基板上に設けられた第３の電極パッドとを備え、
（１）前記第２の配線電極手段は、前記圧電基板上に設けられており、且つ、（２）前記第２及び第３のＩＤＴ電極は不平衡型であって、しかも前記第２の配線電極手段を介して前記第３の電極パッドに接続されており、
前記第１の配線電極手段は、前記回路基板に設けられており、
前記弾性表面波フィルタ素子が、前記回路基板に実装されることにより、前記第１、第２の電極パッドが、前記第１の配線電極手段に接続される請求項６に記載の弾性表面波フィルタ素子。
【請求項９】　前記第３の電極パッドが前記第２のＩＤＴ電極の一方の電極指に接続されており、且つ、前記第４の電極パッドが前記第３のＩＤＴ電極の他方の電極指に接続されており、
前記他方の電極指が、前記一方の電極指から見て逆側に設けられている請求項７に記載の弾性表面波フィルタ素子。
【請求項１０】　前記第２の配線電極手段が、前記第２のＩＤＴ電極の一方の電極指に接続されており、且つ、前記第３のＩＤＴ電極の他方の電極指に接続されており、
前記他方の電極指が、前記一方の電極指から見て逆側に設けられている請求項８に記載の弾性表面波フィルタ素子。
【請求項１１】　前記弾性表面波フィルタ素子は、第１のＩＤＴ電極と、その両側に配置された２つの反射器電極により構成される弾性表面波共振子とを、梯子型又は、対称格子型に接続した構成である請求項１に記載の弾性表面波フィルタ素子。
【請求項１２】　請求項１～１１の何れか一つに記載の弾性表面波フィルタ素子と、
前記弾性表面波フィルタ素子が実装された回路基板と、を備えた弾性表面波フィルタ。
【請求項１３】　前記回路基板がセラミックパッケージの一部を構成している請求項１２に記載の弾性表面波フィルタ。
【請求項１４】　前記回路基板は誘電体により構成され

た積層体であり、
前記弾性表面波フィルタ素子は前記積層体上に実装される構成であって、
前記配線電極手段は、前記積層体最上面に、または前記積層体内層に設けられている請求項１２に記載の弾性表面波フィルタ。
【請求項１５】　前記ＩＤＴ電極と、前記回路基板上に形成された配線電極手段とが空間的に重ならない様に配置されている請求項１２に記載の弾性表面波フィルタ。
【請求項１６】　前記実装がフェースダウン実装である請求項１２に記載の弾性表面波フィルタ。
【請求項１７】　前記異なる平面間は自由空間であることを特徴とする請求項１に記載の弾性表面波フィルタ素子。
【請求項１８】　前記異なる平面間の比誘電率をε、前記異なる平面にそれぞれ形成される前記第１及び第２の配線電極手段間の距離をｔ、前記第１の配線電極手段と、前記第２の配線電極手段との交差部分の面積をＳとした時に、
$\varepsilon \times S / t \leq 1.1 \times 10^{-2}$
を満足する請求項１に記載の弾性表面波フィルタ素子。
【請求項１９】　前記圧電基板は、実効比誘電率が４０以上の基板であることを特徴とする請求項１に記載の弾性表面波フィルタ素子。
【請求項２０】　前記圧電基板の材料が、タンタル酸リチウム及び、ニオブ酸リチウムの中から選ばれたものである請求項１９に記載の弾性表面波フィルタ素子。
【請求項２１】　前記第１の配線電極手段と、前記第２の配線電極手段との寄生成分としてのアドミッタンスの値が０．６ｍＳ以下となるように構成されることを特徴とする請求項１に記載の弾性表面波フィルタ素子。
【請求項２２】　請求項１～１１、１７～２１の何れか一つに記載の弾性表面波フィルタ素子と、
所定の半導体装置と、
前記弾性表面波フィルタ素子及び前記半導体装置が実装された基板と、を備えたモジュール。
【請求項２３】　前記基板は、誘電体層が積層された積層体である請求項２２記載のモジュール。
【請求項２４】　前記半導体装置が、低雑音増幅器である請求項２２に記載のモジュール。
【請求項２５】　前記低雑音増幅器が平衡型である請求項２４に記載のモジュール。
【請求項２６】　前記半導体装置が、スイッチ素子であるか、又はミキサーである請求項２４に記載のモジュール。
【請求項２７】　（１）圧電基板と、（２）前記圧電基板上に形成された複数のインターディジタルトランスデューサ電極（ＩＤＴ電極）とを有する弾性表面波フィルタ素子と、
前記弾性表面波フィルタ素子が実装された回路基板と、
前記複数のＩＤＴ電極の内、少なくとも一つのＩＤＴ電極を、前記回路基板に設けられた平衡型端子に接続するための第１の配線電極手段と、
前記複数のＩＤＴ電極の内、他のＩＤＴ電極を、前記回路基板に設けられた平衡型端子または不平衡型端子に接続するための第２の配線電極手段とを備え、
前記第１の配線電極手段と、前記第２の配線電極手段とが、互いに異なる平面上に配置されている弾性表面波フィルタ。
【請求項２８】　アンテナと、
前記アンテナに接続されたスイッチ手段と、
前記スイッチ手段と送信回路の間に設けられた送信フィルタと、
前記スイッチ手段と受信回路の間に設けられた受信フィルタとを備えた通信機器であって、
前記送信フィルタ及び／又は前記受信フィルタが、請求項１～１１，１７～２１，２７の何れか一つに記載の弾性表面波フィルタ素子を有している通信機器。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、電気的特性の劣化を抑えた平衡型端子を有する弾性表面波フィルタ素子、弾性表面波フィルタ、モジュール、及び通信機器に関するものである。
【０００２】
【従来の技術】近年、移動体通信の発展に伴い、使用される部品の高性能化、小型化が期待されている。さらに、対雑音特性の良好化を目的としてＩＣなどの半導体部品の平衡化が進み、ＲＦ段に使用される弾性表面波フィルタ素子においても平衡化が求められている。
【０００３】従来より、移動体通信機器などのＲＦ段のフィルタとしては、弾性表面波フィルタが広く用いられている。特に、縦モード型の弾性表面波フィルタ素子は平衡－不平衡変換が容易に実現できる。
【０００４】さらには、小型化に関して、従来のワイヤーボンディング実装技術からフリップチップやＣＳＰ（Chip Size Package）などに代表されるフェースダウン実装技術が主流となりつつある。
【０００５】以下、従来の平衡型入出力端子を有する縦モード型の弾性表面波フィルタ素子について説明する。
【０００６】図７に従来の平衡型端子を有する縦モード型の弾性表面波フィルタの構成を示す。
【０００７】図７において、弾性表面波フィルタ素子は、圧電基板７０１上に、第１、第２、第３のインターディジタルトランスデューサ電極（以下、ＩＤＴ電極と称する）７０２、７０３、７０４と第１、第２の反射器電極７０５、７０６とにより構成される。第１のＩＤＴ電極７０２の一方の電極指は平衡型端子の一方７０７に接続され、第１のＩＤＴ電極７０２の他方の電極指は平衡型端子の他方７０８に接続される。

【０００８】また、第２、第３のＩＤＴ電極７０３、７０４の一方の側の電極指を不平衡型端子７０９に接続し、他方を接地する。以上の構成とすることにより不平衡型－平衡型端子を有する弾性表面波フィルタ素子が得られる。

【０００９】次に、前記弾性表面波フィルタ素子を回路基板上にフェースダウン実装する場合の構成についての一例を述べる。図８（ａ）は、図７の弾性表面波フィルタ素子の圧電基板上の構成を模式的に示した図である。

【００１０】第１のＩＤＴ電極７０２の一方の電極指は第１の配線電極８０１を介して第１の電極パッド８０２に接続される。第１のＩＤＴ電極７０２の他方の電極指は第２の配線電極８０３を介して第２の電極パッド８０４に接続される。

【００１１】第２のＩＤＴ電極７０３の一方の側の電極指と、第３のＩＤＴ電極７０４の一方の側の電極指は、それぞれ第３の配線電極８０５を介して第３の電極パッド８０６に接続される。また、接地電極に関しては省略している。

【００１２】図８（ｂ）に示すのは、前述の弾性表面波フィルタ素子が実装される回路基板の表層図である。回路基板８０７には第１の回路基板上配線電極８０８、第２の回路基板上配線電極８０９、第３の回路基板上配線電極８１０がそれぞれ設けられている。

【００１３】図８（ａ）に示す弾性表面波フィルタ素子は、回路基板８０７に対向するように実装される。例えば、金バンプを用いた超音波熱圧着による実装方法を用いることができる。この時、第１の電極パッド８０２は第１の回路基板上配線電極８０８に接続され、第２の電極パッド８０４は第２の回路基板上配線電極８０９に接続され、第３の電極パッド８０６は第３の回路基板上配線電極８１０に接続される。

【００１４】第１、第２、第３の回路基板上配線電極８０８、８０９、８１０は、スルーホールやビアホール、或いは回路基板の外部の電極などにより端子として引き出される。この場合、第１、第２、第３の電極８０８、８０９、８１０はそれぞれ、平衡型出力端子の一方ＯＵＴ１、平衡型出力端子の他方ＯＵＴ２、不平衡型入力端子ＩＮに接続され、不平衡型－平衡型端子を有する弾性表面波フィルタが実現される。

【００１５】又、従来の弾性表面波デバイスは、弾性表面波素子の接地用電極パッドの少なくとも１つと、表面実装用パッケージの接地用外部接続端子の少なくとも１つとを接続する接地用連絡導体を、表面実装用パッケージ内面に複数設けることにより、帯域外抑圧度を向上している（例えば、特許文献１参照。）。

【００１６】又、従来の弾性表面波デバイスは、不平衡型入力端子と平衡型ＩＤＴの端子間に結合があると同相電圧が発生するので、両ＩＤＴ間の電気的結合は出来るだけ抑圧しなければならないと示されているが、その具体的構成に関しては開示されていない（例えば、非特許文献１参照。）。

【００１７】

【特許文献１】特開平１１－１４５７７２号公報

【非特許文献１】「２００１年電子情報通信学会基礎・境界ソサイエティ大会講演論文集」社団法人電子情報通信学会、２００１年８月２９日、ｐ２８３－２８４

【００１８】

【発明が解決しようとする課題】しかしながら、上述の弾性表面波フィルタ素子あるいは、弾性表面波フィルタにおいては、重要な電気的特性の一つであるバランス特性に関して、その劣化の原因に関する詳細な議論が少なく、バランス特性を考慮した圧電基板上の配線電極構成、そして回路基板の構造が明確化されていなかった。

【００１９】本発明では、上記従来のこの様な課題を考慮して、平衡型端子を有する弾性表面波フィルタ素子あるいは、弾性表面波フィルタに関して、バランス特性の劣化原因を明確化し、その改善を行い、良好なバランス特性を有する弾性表面波フィルタ素子、弾性表面波フィルタ、モジュール、及び通信機器を提供することを目的とするものである。

【００２０】

【課題を解決するための手段】第１の本発明は、圧電基板（例えば、符号１０１）と、前記圧電基板上に形成された複数のインターディジタルトランスデューサ電極（以下、ＩＤＴ電極と称す）（例えば、符号１０２，１０３，１０４）とを備えた弾性表面波フィルタ素子であって、前記複数のＩＤＴ電極（例えば、符号１０２，１０３，１０４）の内、少なくとも一つのＩＤＴ電極（例えば、符号１０２）は平衡型端子に接続され、他のＩＤＴ電極（例えば、符号１０３，１０４）は平衡型端子または不平衡型端子に接続され、前記少なくとも一つのＩＤＴ電極（例えば、符号１０２）に接続されるべき又は接続された第１の配線電極手段（例えば、符号１０７，１０９）と、前記他のＩＤＴ電極に接続されるべき又は接続された第２の配線電極手段（例えば、符号１１６）とが、互いに異なる平面上に配置されている弾性表面波フィルタ素子である。

【００２１】第２の本発明は、前記第１及び第２の配線電極手段の内、一方の前記配線電極手段が前記圧電基板の主面上に配置されており、他の前記配線電極手段は前記圧電基板が実装されるべき回路基板（例えば、符号１１３）上に配置されている上記第１の本発明の弾性表面波フィルタ素子である。

【００２２】第３の本発明は、（１）前記第１及び第２の配線電極手段の内、一方の前記配線電極手段が前記圧電基板上に形成されており、且つ、他方の前記配線電極手段は前記圧電基板が実装されるべき回路基板の内層電極である、又は、（２）前記第１及び第２の配線電極手段の内、一方の前記配線電極手段は前記圧電基板が実装

されるべき回路基板上に形成され、且つ、他方の前記配線電極手段は前記回路基板の内層電極である上記第１の本発明の弾性表面波フィルタ素子である。

【００２３】第４の本発明は、前記第１及び第２の配線電極手段の内、一方の前記配線電極手段が圧電基板の主面上に設けられており、他方の前記配線電極手段が前記圧電基板の前記主面上に形成された保護膜（例えば、符号１９０２）上に設けられている上記第１の本発明の弾性表面波フィルタ素子である。

【００２４】第５の本発明は、前記保護膜が誘電体薄膜である上記第４の本発明の弾性表面波フィルタ素子である。

【００２５】第６の本発明は、前記弾性表面波フィルタ素子が、第１、第２、第３のＩＤＴ電極（例えば、符号１０２，１０３，１０４）と少なくとも２つの反射器電極（例えば、符号１０５，１０６）とを弾性表面波の伝搬方向に沿って配置した縦モード型の弾性表面波フィルタ素子であって、前記第１のＩＤＴ電極の両側に前記第２、第３のＩＤＴ電極が配置される構成である上記第１の本発明の弾性表面波フィルタ素子である。

【００２６】第７の本発明は、前記圧電基板上に設けられた第１及び第２の電極パッド（例えば、図１（ａ）中の符号１０８，１１０）と、前記圧電基板上に設けられた、前記第２のＩＤＴ電極に実質上直接に接続された第３の電極パッド（例えば、図１（ａ）中の符号１１１）と、前記圧電基板上に設けられた、前記第３のＩＤＴ電極に実質上直接に接続された第４の電極パッド（例えば、図１（ａ）中の符号１１２）とを備え、（１）前記第１の配線電極手段手段は、一対の配線電極（例えば、符号１０７と１０９）として前記圧電基板上に設けられており、且つ、（２）前記第１のＩＤＴ電極（例えば、符号１０２）は、平衡型であって、しかも前記一対の配線電極（例えば、符号１０７と１０９）の各配線電極を介して前記第１、第２の電極パッド（例えば、符号１０８，１１０）に接続されており、前記第２の配線電極手段（例えば、符号１１６）は、前記回路基板（例えば、符号１１３）に設けられており、前記弾性表面波フィルタ素子が、前記回路基板に実装されることにより、前記第３、第４の電極パッド（例えば、符号１１１，１１２）が、前記第２の配線電極手段（例えば、符号１１６）に接続される上記第６の本発明の弾性表面波フィルタ素子である。

【００２７】第８の本発明は、前記圧電基板上に設けられた、前記第１のＩＤＴ電極に実質上直接に接続された第１及び第２の電極パッド（例えば、図３（ａ）中の符号１０８，１１０）と、前記圧電基板（例えば、符号１０１）上に設けられた第３の電極パッド（例えば、図３（ａ）中の符号３０２）とを備え、（１）前記第２の配線電極手段（例えば、図３（ａ）中の符号３０１）は、前記圧電基板上に設けられており、且つ、（２）前記第２及び第３のＩＤＴ電極（例えば、図３（ａ）中の符号１０３，１０４）は不平衡型であって、しかも前記第２の配線電極手段（例えば、符号３０１）を介して前記第３の電極パッド（例えば、符号３０２）に接続されており、前記第１の配線電極手段（例えば、図３（ｂ）中の符号３０３，３０４）は、前記回路基板（例えば、図３（ｂ）中の符号１１３）に設けられており、前記弾性表面波フィルタ素子が、前記回路基板に実装されることにより、前記第１、第２の電極パッドが、前記第１の配線電極手段に接続される上記第６の本発明の弾性表面波フィルタ素子である。

【００２８】第９の本発明は、前記第３の電極パッド（例えば、図５（ａ）中の符号５０５）が前記第２のＩＤＴ電極（例えば、図５（ａ）中の４０３）の一方の電極指（例えば、図５（ａ）中の符号４０３ａ）に接続されており、且つ、前記第４の電極パッド（例えば、図５（ａ）中の符号５０６）が前記第３のＩＤＴ電極（例えば、図５（ａ）中の符号４０４）の他方の電極指に接続されており、前記他方の電極指が、前記一方の電極指から見て逆側に設けられている上記第７の本発明の弾性表面波フィルタ素子である。

【００２９】第１０の本発明は、前記第２の配線電極手段（例えば、図１５（ａ）中の符号３０１１）が、前記第２のＩＤＴ電極（例えば、図１５（ａ）中の符号１０３）の一方の電極指（例えば、図１５（ａ）中の符号１０３ａ）に接続されており、且つ、前記第３のＩＤＴ電極（例えば、図１５（ａ）中の符号１０４）の他方の電極指（例えば、図１５（ａ）中の符号１０４ａ）に接続されており、前記他方の電極指（例えば、図１５（ａ）中の符号１０４ｂ）が、前記一方の電極指（例えば、図１５（ａ）中の符号１０３ａ）から見て逆側に設けられている上記第８の本発明の弾性表面波フィルタ素子である。

【００３０】第１１の本発明は、前記弾性表面波フィルタ素子は、第１のＩＤＴ電極と、その両側に配置された２つの反射器電極により構成される弾性表面波共振子とを、梯子型又は、対称格子型に接続した構成である上記第１の本発明の弾性表面波フィルタ素子である。

【００３１】第１２の本発明は、上記第１～１１の何れか一つの本発明の弾性表面波フィルタ素子と、前記弾性表面波フィルタ素子が実装された回路基板と、を備えた弾性表面波フィルタである。

【００３２】第１３の本発明は、前記回路基板がセラミックパッケージの一部を構成している上記第１２の本発明の弾性表面波フィルタである。

【００３３】第１４の本発明は、前記回路基板は誘電体により構成された積層体であり、前記弾性表面波フィルタ素子は前記積層体上に実装される構成であって、前記配線電極手段は、前記積層体最上面に、または前記積層体内層に設けられている上記第１２の本発明の弾性表面

波フィルタである。

【００３４】第１５の本発明は、前記ＩＤＴ電極と、前記回路基板上に形成された配線電極手段とが空間的に重ならない様に配置されている上記第１２の本発明の弾性表面波フィルタである。

【００３５】第１６の本発明は、前記実装がフェースダウン実装である上記第１２の本発明の弾性表面波フィルタである。

【００３６】第１７の本発明は、前記異なる平面間は自由空間であることを特徴とする上記第１の本発明の弾性表面波フィルタ素子である。

【００３７】第１８の本発明は、前記異なる平面間の比誘電率をε、前記異なる平面にそれぞれ形成される前記第１及び第２の配線電極手段間の距離をｔ、前記第１の配線電極手段と、前記第２の配線電極手段との交差部分の面積をＳとした時に、

$\varepsilon \times S / t \leq 1.1 \times 10^{-2}$

を満足する上記第１の本発明の弾性表面波フィルタ素子である。

【００３８】第１９の本発明は、前記圧電基板は、実効比誘電率が４０以上の基板であることを特徴とする上記第１の本発明の弾性表面波フィルタ素子である。

【００３９】第２０の本発明は、前記圧電基板の材料が、タンタル酸リチウム及び、ニオブ酸リチウムの中から選ばれたものである上記第１９の本発明の弾性表面波フィルタ素子である。

【００４０】第２１の本発明は、前記第１の配線電極手段と、前記第２の配線電極手段との寄生成分としてのアドミッタンスの値が０．６ｍＳ以下となるように構成されることを特徴とする上記第１の本発明の弾性表面波フィルタ素子である。

【００４１】第２２の本発明は、上記第１～１１、１７～２１の何れか一つの本発明の弾性表面波フィルタ素子と、所定の半導体装置と、前記弾性表面波フィルタ素子及び前記半導体装置が実装された基板と、を備えたモジュールである。

【００４２】第２３の本発明は、前記基板は、誘電体層が積層された積層体である上記第２２記載のモジュールである。

【００４３】第２４の本発明は、前記半導体装置が、低雑音増幅器である上記第２２の本発明のモジュールである。

$$\sqrt{\{(\varepsilon_{11}^{T}) \times (\varepsilon_{33}^{T})\}}$$

【００４４】第２５の本発明は、前記低雑音増幅器が平衡型である上記第２４の本発明のモジュールである。

【００４５】第２６の本発明は、前記半導体装置が、スイッチ素子であるか、又はミキサーである上記第２４の本発明のモジュールである。

【００４６】第２７の本発明は、（１）圧電基板と、（２）前記圧電基板上に形成された複数のインターディジタルトランスデューサ電極（ＩＤＴ電極）とを有する弾性表面波フィルタ素子と、前記弾性表面波フィルタ素子が実装された回路基板と、前記複数のＩＤＴ電極の内、少なくとも一つのＩＤＴ電極を、前記回路基板に設けられた平衡型端子に接続するための第１の配線電極手段と、前記複数のＩＤＴ電極の内、他のＩＤＴ電極を、前記回路基板に設けられた平衡型端子または不平衡型端子に接続するための第２の配線電極手段とを備え、前記第１の配線電極手段と、前記第２の配線電極手段とが、互いに異なる平面上に配置されている弾性表面波フィルタである。

【００４７】第２８の本発明は、アンテナと、前記アンテナに接続されたスイッチ手段と、前記スイッチ手段と送信回路の間に設けられた送信フィルタと、前記スイッチ手段と受信回路の間に設けられた受信フィルタとを備えた通信機器であって、前記送信フィルタ及び／又は前記受信フィルタが、上記第１～１１，１７～２１，２７の何れか一つの本発明の弾性表面波フィルタ素子を有している通信機器である。

【００４８】

【発明の実施の形態】（実施の形態１）以下、本発明の実施の形態１の弾性表面波フィルタ素子、及び弾性表面波フィルタについて図面を参照しながら説明する。

【００４９】まず、前述の弾性表面波フィルタ素子のバランス特性の劣化原因に関しての考察を行う。図９に示すのは、図８（ａ）の弾性表面波フィルタにおいてＡ－Ａ’で切り出した断面図である。このような弾性表面波は一般的にリチウム酸タンタル（$LiTaO_3$）やリチウム酸ニオブ（$LiNbO_3$）などの圧電基板が広く用いられており、このような基板の実効比誘電率はそれぞれ４８、４９程度と大きい値である。ここで、実効比誘電率とは圧電基板の比誘電率テンソルε_{11}^{T}とε_{33}^{T}を用いて、次式１の通り定義する。

【００５０】

【数１】

図９に示すように、第１の配線電極８０１と第３の配線電極８０５の間には基板を介する寄生成分Ｃｓｕｂ、空間的な寄生成分Ｃｐなどが生じる。

【００５１】圧電基板上で配線電極を用いて配線を行う場合には比誘電率が大きいので、その影響も大きくなる。また、これらの電極の距離を離せば、寄生成分による結合は小さくできるが、実際には弾性表面波フィルタ素子の小型化も同時に必要であり、これらの電極の距離を大きくするのには限界がある。

【００５２】図１０に、これらの寄生成分を考慮した構成を示す。図７の弾性表面波フィルタにおける寄生成分としては、入出力ＩＤＴ電極間に容量成分１００１を仮

定した構成が考えられる。図１０に示す構成で容量成分１００１の容量値を変化させて、９００ＭＨｚ帯のフィルタに関して解析を行った結果を図１１（ａ）、図１１（ｂ）に示す。

【００５３】図１１（ａ）、図１１（ｂ）はバランス特性を表す指標として、振幅バランス特性、位相バランス特性を示した図である。

【００５４】ここで、振幅バランス特性とは次の通りである。即ち、図７又は図１０に示す弾性表面波フィルタ素子の不平衡型端子７０９から入力された信号は、平衡型端子の一方の７０７と他方の７０８にバランス信号として出力される。その場合の平衡型端子の一方の７０７に出力される信号振幅と、平衡型端子の他方の７０８に出力される信号振幅との振幅差を表したものが、振幅バランス特性である。そして、この値が零となればバランス特性の劣化はないといえる。

【００５５】又、位相バランス特性とは、上記平衡型端子の一方の７０７に出力される信号の位相と、上記平衡型端子の他方の７０８に出力される信号の位相との位相差の１８０度からのずれを表したものである。そして、この値が零となればバランス特性の劣化はないといえる。

【００５６】図１１（ａ）、図１１（ｂ）は、通過帯域内における振幅、位相のバランス特性の最大値と最小値を示している。図１１（ａ）が振幅バランス特性であり、図１１（ｂ）が位相バランス特性である。

【００５７】図１１（ａ）、図１１（ｂ）に示すように、容量値が大きくなる程バランス特性が劣化している。即ち、入出力間の寄生成分による結合が大きい程バランス特性が劣化する。

【００５８】振幅バランス特性を±１ｄＢ以内、位相バランス特性を±１０度以内のフィルタを実現するには、入出力間の寄生成分としての容量値を０．１０ｐＦ以下にする必要がある。即ち、アドミッタンス成分Ｙで考えるとＹ＝２πｆＣより、Ｙが０．６［ｍＳ］以下とすればよい。ここでｆは周波数、Ｃは容量値である。

【００５９】次に、前述のバランス特性の劣化原因を克服する弾性表面波フィルタ素子、及び弾性表面波フィルタの構成について述べる。

【００６０】図１（ａ）は、弾性表面波フィルタ素子の圧電基板上の構成を模式的に示した図である。第１のＩＤＴ電極１０２の一方の電極指は第１の配線電極１０７を介して第１の電極パッド１０８に接続される。

【００６１】第１のＩＤＴ電極１０２の他方の電極指は第２の配線電極１０９を介して第２の電極パッド１１０に接続される。

【００６２】第２、第３のＩＤＴ電極１０３、１０４の一方の側の電極指は実質上直接に第３、第４の電極パッド１１１、１１２に接続される。第２、第３のＩＤＴ電極１０３、１０４の他方の側の電極指は接地されるが、ここでは接地電極に関しては省略している。

【００６３】図１（ｂ）に示すのは、前述の弾性表面波フィルタ素子が実装される回路基板の表層図である。回路基板１１３には第１、第２、第３の回路基板上配線電極１１４、１１５、１１６が設けられている。

【００６４】図１（ａ）に示す弾性表面波フィルタ素子は、回路基板１１３に対向するように実装される（図１２参照）。ここで、図１２は、弾性表面波フィルタ素子が回路基板１１３に対向するように実装された弾性表面波フィルタの分解斜視図である。

【００６５】例えば、金バンプを用いた超音波熱圧着による実装方法を用いることができる。

【００６６】この時、第１の電極パッド１０８は第１の回路基板上配線電極１１４に接続され、第２の電極パッド１１０は第２の回路基板上配線電極１１５に接続され、第３、第４の電極パッド１１１、１１２は第３の回路基板上配線電極１１６の２箇所に接続される。

【００６７】この時、回路基板上の配線電極１１６は、図８（ａ）の第３の配線電極８０５と同じ役割、即ち、第３の電極パッド１１１と第４の電極パッド１１２とを電気的に接続するための配線電極としての役割を担う。

【００６８】第１、第２、第３の回路基板上配線電極１１４、１１５、１１６はスルーホールやビアホール、或いは回路基板の外部の電極などにより端子として引き出される。

【００６９】この場合、第１、第２、第３の電極１１４、１１５、１１６はそれぞれ、平衡型出力端子の一方ＯＵＴ１、平衡型出力端子の他方ＯＵＴ２、不平衡型入力端子ＩＮに接続され、不平衡型－平衡型端子を有する弾性表面波フィルタが実現される。

【００７０】以上の構成とすることにより、第１のＩＤＴ電極における第１、第２の配線電極１０７、１０９と第２、第３のＩＤＴ電極に接続される第３の回路基板上の配線電極１１６は空間的に離れた配置となる。

【００７１】この様な構成によれば、図８（ａ）に示す構成と比べて、明らかに入出力間での結合を最小限に抑えることができ、弾性表面波フィルタ素子のバランス特性を改善することができる。

【００７２】尚、本発明の第１の配線電極手段は、図１（ａ）の第１、第２の配線電極１０７，１０９で表された一対の配線電極に対応する。又、本発明の第２の配線電極手段は、図１（ｂ）に示す第３の回路基板上配線電極１１６に対応する。

【００７３】また、図２において、第１の配線電極１０７と第３の回路基板上の配線電極１１６とは交差する部分が生じるが、この部分での寄生成分Ｃａは、交差部分を近似的に平行平板コンデンサとして仮定すると、次式２で表される。

【００７４】

【数２】$Ca=\varepsilon_0\times S/t$となる。

【００７５】ここで、ε_0は自由空間の誘電率であり、Ｓは交差部分の面積、ｔは電極間の距離である。

【００７６】例えば、Ｓ＝１００μｍ×１００μｍ、ｔ＝２０μｍとすると、式２より、Ｃａは４．４［ｆＦ］と小さな値となる。

【００７７】なお、実際には交差部分以外の要素も考慮して、圧電基板、回路基板の構成を最適化する必要があるが、空間的に離れた配置であれば、従来よりも入出力間の結合を小さくすることができ、バランス特性が改善するという効果は同様に得られる。

【００７８】また、弾性表面波フィルタ素子の圧電基板上の配線電極をなくして、回路基板を多層基板とし配線を行う場合には、基板を含めたフィルタ全体の高さは若干高くなるので、低背化を考えた場合には欠点となるが、バランス特性に関しては、小さい比誘電率の基板であれば、改善の効果がある。

【００７９】例えば、回路基板としてはアルミナやセラミック誘電体からなる積層体などが挙げられ、これらの比誘電率は１０程度のものがある。この場合、前式においてはＣａは０．０４［ｐＦ］となり、図１１より、バランス特性の劣化が小さいことが分かる。

【００８０】よって、これらの回路基板内での多層配線を行って、寄生成分が０．１ｐＦ以下になるような構成とするには、回路基板材料の比誘電率εと配線電極間の距離ｔ、配線電極の交差部分の面積Ｓとの関係が

【００８１】

【数３】$\varepsilon \times S / t \leqq 1.1 \times 10^{-2}$

を満たすことが好ましい。

【００８２】但し、複数の異なる比誘電率の材料が平面間に存在する場合には、平面間全体で上記の関係を満足すればよい。

【００８３】また、本実施の形態においては、平衡側の配線電極１０７、１０９を圧電基板１０１の上に形成し、不平衡側は回路基板上の回路基板上の配線電極１１６と実質上直接に接続している。しかしこれに限らず例えば、図３に示すように、不平衡側の第２、第３のＩＤＴ電極１０３、１０４は配線電極３０１を介して、電極パッド３０２に接続して、第１、第２の電極パッド１０８、１１０は第１のＩＤＴ電極１０２に実質上直接に接続される構成としても構わない。

【００８４】この時、第１、第２の電極パッド１０８、１１０は回路基板上の配線電極３０３、３０４に接続される。従って、回路基板上の配線電極３０３は、図８（ａ）の第１の配線電極８０１と同様の配線電極としての役割を担う。また、回路基板上の配線電極３０４は、図８（ａ）の第２の配線電極８０３と同様の配線電極としての役割を担う。

【００８５】また、第３の電極パッド３０２は回路基板上の配線電極３０５に接続される。この場合は、回路基板１１３の表層の配置される回路基板上の配線電極３０３，３０４，３０５は圧電基板１０１上の弾性表面波の構成に応じて適宜配置されるものである。

【００８６】以上の構成においても、第１のＩＤＴ電極における第１、第２の回路基板上の配線電極３０３，３０４と第２、第３のＩＤＴ電極の配線電極３０１は空間的に離れた配置となり、入出力間での結合を最小限に抑えることができ、弾性表面波フィルタのバランス特性を改善することができる。

【００８７】尚、本発明の第１の配線電極手段は、図３（ｂ）の第１、第２の回路基板上配線電極３０３，３０４に表された一対の配線電極に対応する。又、本発明の第２の配線電極手段は、図３（ａ）に示す配線電極３０１に対応する。

【００８８】なお、本実施形態においては、回路基板として説明したが、これはパッケージなどであっても構わない。

【００８９】又、本実施の形態においては、第２，第３のＩＤＴ電極１０３，１０４の一方の側の電極指は、実質上直接に第３，第４の電極パッド１１１，１１２に接続される構成について説明したが、これに限らず、例えば、バスバー電極等を介して接続されていてもよく、配線の長さが短くなるような構成で最適化されていればよい。

【００９０】（実施の形態２）以下、本発明の実施の形態２の弾性表面波フィルタ素子及び弾性表面波フィルタについて図面を参照して説明する。

【００９１】図４において、弾性表面波フィルタ素子は、圧電基板４０１上に、第１、第２、第３のＩＤＴ電極４０２、４０３、４０４と第１、第２の反射器電極４０５、４０６と、ＩＤＴ電極と反射器電極とにより構成される弾性表面波共振子４１０とにより構成される。

【００９２】第１のＩＤＴ電極４０２の一方の電極指は平衡型端子の一方４０７に接続され、第１のＩＤＴ電極４０２の他方の電極指は平衡型端子の他方４０８に接続される。

【００９３】また、不平衡型端子４０９は、弾性表面波共振子４１０を介して第２のＩＤＴ電極４０３の一方の側の電極指４０３ａと第３のＩＤＴ電極４０４の他方の電極指４０４ｂとに接続される。

【００９４】ここで、第２のＩＤＴ電極４０３の一方の側の電極指４０３ａと第３のＩＤＴ電極４０４の他方の電極指４０４ｂとは、図４、図５に示す様に、一方から見て他方が逆側に配置されている電極指である。

【００９５】以上の構成とすることにより不平衡型－平衡型端子を有する弾性表面波フィルタ素子が得られる。

【００９６】次に、前記弾性表面波フィルタ素子をパッケージや基板上にフェースダウン実装する場合の構成についての一例を述べる。図５（ａ）は、弾性表面波フィルタ素子の圧電基板上の構成を模式的に示した図である。

【００９７】第１のＩＤＴ電極４０２の一方の電極指は第１の配線電極５０１を介して第１の電極パッド５０２に接続される。第１のＩＤＴ電極４０２の他方の電極指は第２の配線電極５０３を介して第２の電極パッド５０４に接続される。

【００９８】第２のＩＤＴ電極４０３の一方の側の電極指は実質上直接に第３の電極パッド５０５に接続される。第３のＩＤＴ電極４０４の他方の側の電極指は実質上直接に第４の電極パッド５０６に接続される。

【００９９】第２のＩＤＴ電極４０３の他方の側の電極指、第３のＩＤＴ電極４０４の一方の側の電極指は接地されるが、ここでは接地電極に関してはその記載を省略している。

【０１００】さらに、弾性表面波共振器４１０のＩＤＴ電極の一方と他方には第５、第６の電極パッド５０７、５０８に実質上直接に接続される。

【０１０１】図５（ｂ）に示すのは、前述の弾性表面波フィルタ素子が実装される回路基板の表層図である。回路基板５０９には第１、第２、第３、第４の回路基板上配線電極５１０、５１１、５１２、５１３が設けられている。

【０１０２】図５（ａ）に示す弾性表面波フィルタ素子は、回路基板５０９に対向するように実装される。

【０１０３】例えば、金バンプを用いた超音波熱圧着による実装方法を用いることができる。この時、第１の電極パッド５０２は第１の回路基板上配線電極５１０に接続され、第２の電極パッド５０４は第２の回路基板上配線電極５１１に接続され、第３、第４の電極パッド５０５、５０６は第３の回路基板上配線電極５１２に接続される。

【０１０４】また、第５の電極パッド５０７は第４の回路基板上配線電極５１３に接続され、第６の電極パッド５０８は第３の回路基板上配線電極５１２に接続される。

【０１０５】即ち、第３の回路基板上配線電極５１２には３箇所の電極パッドが接続されていて、弾性波共振器４１０と第２、第３のＩＤＴ電極４０３、４０４を接続する配線電極の役割を担っている。

【０１０６】また、第１、第２、第４の回路基板上配線電極５１０、５１１、５１３はスルーホールやビアホール、或いは回路基板の外部の電極などにより端子として引き出される。

【０１０７】この場合、第１、第２、第４の電極５１０、５１１、５１３はそれぞれ、平衡型出力端子の一方ＯＵＴ１、平衡型出力端子の他方ＯＵＴ２、不平衡型入力端子ＩＮに接続され、不平衡型－平衡型端子を有する弾性表面波フィルタが実現される。

【０１０８】以上の構成とすることにより、第１のＩＤＴ電極における第１、第２の配線電極５０１、５０３と第２、第３のＩＤＴ電極に接続される第３の回路基板上配線電極５１２は空間的に離れた配置となり、入出力間での結合を最小限に抑えることができ、弾性表面波フィルタ素子のバランス特性を改善することができる。

【０１０９】実際に、本発明のフィルタと従来の構成のフィルタとの実測結果を比較してみたところ、１．８ＧＨｚ帯のフィルタにてバランス特性を評価したところ、本発明の構成とすることにより、振幅、及び位相バランス特性の偏差（最大値と最小値との差）が２５％程度改善される結果が得られた。

【０１１０】さらに、回路基板上の配線電極と圧電基板上に形成されるＩＤＴ電極とが空間的に重ならない構成とすることによって、さらに寄生成分を小さくすることができる。

【０１１１】即ち、図６中に示す矢印Ａの方向に沿って圧電基板４０１を見た場合、図６に示すように、ＩＤＴ電極６０１と回路基板上の配線電極６０２とが重ならない構成とすることが有効である。仮に図６の破線で示した部分６０３に回路基板上の配線電極を設けてしまうとＩＤＴ電極との間に寄生成分６０４が生じ、電気特性の劣化の原因となる。

【０１１２】尚、上記実施の形態では、本発明の第１、第２の配線電極の内、何れか一方の配線電極が圧電基板上に設けられ、他の配線電極が回路基板上に設けられている例を中心に述べた。

【０１１３】しかしこれに限らず例えば、（１）前記第１及び第２の配線電極の内、一方の前記配線電極が前記圧電基板上に形成されており、且つ、他方の前記配線電極は前記圧電基板が実装されるべき回路基板の内層電極である構成でも良いし（図１３参照）、あるいは、（２）前記第１及び第２の配線電極の内、一方の前記配線電極は前記圧電基板が実装されるべき回路基板上に形成され、且つ、他方の前記配線電極は前記回路基板の内層電極である構成（図示省略）でもかまわない。

【０１１４】ここで、図１３は、前者の構成例の分解斜視図であり、図１２の場合と異なり、本発明の第２の配線電極に対応する配線電極が、内層電極１３０１として回路基板の内層面に形成されている。内層電極１３０１は、ビア１３０２を介して第３，第４の電極パッド１１１，１１２と接続されている。尚、端子電極１３０３ａ、１３０３ｂは、回路基板上の表層電極１１４，１１５と電気的に接続されている。又、後者の例としては、例えば、図１３を代用して説明すると、図１３に示す本発明の第１の配線電極手段に対応する第１，第２の配線電極１０７，１０９が、圧電基板上ではなく、回路基板上に表層電極として形成された構成でもよい。あるいは、図１３を代用して説明した上記構成では、本発明の第１の配線電極手段と第２の配線電極手段が、表層電極と内層電極の関係にある場合を示しているが、これら双方の関係が互いに逆の構成、即ち、本発明の第１の配線電極手段が回路基板の内層電極として、且つ本発明の第

２の配線電極手段が回路基板の表層電極として構成されていても良い。

【０１１５】尚、図１４は、図１３の構成例を模式的に表した図である。同図において、圧電基板１０１と回路基板１１３は、便宜上、透明なものとして透過的に表している。又、図中の斜線部は、弾性表面波フィルタ電極部の配置位置を略示したものである。

【０１１６】又、上記実施の形態では、図５（ａ）を用いて、第３の電極パッド５０５が、第２のＩＤＴ電極４０３の一方の電極指４０３ａに接続されており、且つ、第４の電極パッド５０６が、第３のＩＤＴ電極４０４の他方の電極指４０４ｂに接続されており、しかも、その他方の電極指４０４ｂが上記一方の電極指４０３ａから見て逆側に設けられている場合について説明した。

【０１１７】しかしこれに限らず例えば図１５（ａ）に示す様に、本発明の第２の配線電極手段３０１１の一端１５０１ａが、第２のＩＤＴ電極１０３の一方の電極指１０３ａに接続されており、且つ、前記第２の配線電極手段３０１１の他端１５０１ｂが、第３のＩＤＴ電極１０４の他方の電極指１０４ｂに接続されており、且つ、その他方の電極指１０４ｂが上記一方の電極指１０３ａから見て逆側に設けられている弾性表面波フィルタ素子であっても良い。

【０１１８】この場合でも上記実施の形態と同様の効果を発揮する。図１５（ａ）は、図３（ａ）に示した本発明の一実施の形態の弾性表面波フィルタ素子の変形例の構成を示す模式図である。又、図１５（ｂ）は、図１５（ａ）に示す変形例に対応する回路基板の表層図である。

【０１１９】又、上記実施形態においては、圧電基板と回路基板とを有する構成を中心に説明したが、これに限らず、例えば、圧電基板とパッケージから弾性表面波フィルタが構成されていてもよい。この場合、例えば、図１６、図１７に示す様に、セラミックパッケージ１６０１、１７０１の下部が回路基板１６０２、１７０２を兼ねている構成であってもよい。図１６において、符号１６０３，１６０４は外部端子を示す。図１７の構成では、内層電極１１６と外部端子（底面電極）１７０４とをビア１７０３により電気的に接続している点が、図１６と異なる。

【０１２０】ここで、図１６、図１７は、圧電基板とパッケージから弾性表面波フィルタを構成した例を説明するための、図１４と同様に透過的に表した模式図である。図中の斜線部は、弾性表面波フィルタ電極部の配置位置を略示したものである。

【０１２１】又、上記実施の形態では、本発明の第１の配線電極手段と、本発明の第２の配線電極手段とが、互いに異なる平面上に配置されている弾性表面波フィルタ素子、及び弾性表面波フィルタの例として、上記異なる平面の具体例として、圧電基板と回路基板を利用する場合（例えば、図１，図３、図５，図１５）、回路基板の表層面と内層面を利用する場合などについて述べた。

【０１２２】しかし、これに限らず例えば図１８，図１９に示す様に、本発明の第１及び第２の配線電極の内、一方の配線電極（図１８（ａ）～図１９（ｃ）の１０７，１０９）が圧電基板（図１８（ｂ）の１１３）の主面上に設けられており、他方の配線電極（図１９（ｃ）の１９０１）が、圧電基板の主面上に形成された保護膜（図１９（ｃ）の１９０２）上に設けられている弾性表面波フィルタ素子でも上記と同様の効果を発揮する。

【０１２３】尚、図１９（ｂ）、図１９（ｃ）に示す様に、配線電極１９０１はビア１９０５を介して、電極１９０３，１９０４と電気的に接続されている。又、電極パッド１０８はビア１９０６を介して、配線電極１０７と電気的に接続されている。

【０１２４】特に、この保護膜に関しては、酸化シリコンや窒化シリコン等の誘電体薄膜を用いることにより、ＩＤＴ電極のパッシベーション効果と同時に、温度特性を改善する効果も得られる。

【０１２５】又、電極パッドの接続はビアに限るものではなく、電気的接続が行えるものであればどのような構成でもよい。

【０１２６】また、本発明の実施形態１、２においては圧電基板の実効比誘電率が大きい程その効果は大きく、$LiTaO_3$や$LiNbO_3$などの実効比誘電率が４０以上の圧電基板であれば十分な効果が得られる。

【０１２７】また、本発明の実施形態１、２においては３電極の縦モード型フィルタを用いて説明したが、これは２電極や４電極、５電極の縦モード型フィルタであっても、本発明の実施形態のように入力側と出力側の結合が小さくなる構成であれば、バランス特性に関して同様の効果が得られる。また、多電極の縦モード型弾性表面波フィルタに限らず、弾性表面波共振子を用いた梯子型や対称格子型のフィルタ構成であっても、同様に入力側と出力側の結合が小さくなる構成であれば、バランス特性に関して同様の効果が得られる。

【０１２８】また、本実施形態では１段の弾性表面波フィルタ素子について説明したが、これは複数の弾性表面波フィルタ素子を多段に縦続接続した構成であっても構わない。

【０１２９】なお、ＩＤＴ電極の個数が増える程、圧電基板上での配線が複雑となり、配線電極間の寄生成分も大きくなるので本発明によるバランス特性改善の効果は大きいと期待できる。

【０１３０】また、本実施形態１、２においては平衡－不平衡型の弾性表面波フィルタ素子、及び平衡－不平衡型の弾性表面波フィルタについて説明したが、平衡－平衡型の弾性表面波フィルタ素子等であっても、同様に入力側と出力側の結合が小さくなる構成であれば、バランス特性に関して同様の効果が得られる。

【０１３１】また、本実施形態１、２においては入力側を不平衡型、出力側を平衡型としているが、これは逆であっても効果は同様である。

【０１３２】また、図２０（ａ）、図２０（ｂ）に示す様に、実装基板２００１上に本発明の弾性表面波フィルタ素子２００２と半導体ＩＣ２００３とを実装してモジュール化することにより、装置全体がコンパクトに出来、しかもバランス特性の劣化による感度劣化を抑えることができる。同図において、符号２００４，２００５は外部端子を示し、符号２００６は整合回路部である。図２０（ａ）はモジュールの平面図であり、図２０（ｂ）は、その構成例を説明するための、図１４と同様に透過的に表した模式図である。図中の斜線部は、弾性表面波フィルタ電極部の配置位置を略示したものである。

【０１３３】又、上記モジュールにおいて、半導体装置が、低雑音増幅器である構成でも良い。又、上記半導体装置が、ミキサーである構成でもよい。又、半導体を平衡型として説明したが、これは、ＧａＡｓスイッチやＰＩＮダイオードを用いたスイッチなどの様に不平衡－不平衡型のデバイスと、不平衡－平衡型ＳＡＷフィルタを一体化しても良い。

【０１３４】また、本発明の弾性表面波フィルタ素子、又は弾性表面波フィルタを図２１に示す様な平衡型高周波回路を有する通信機器等に適用することが出来る。これにより、送信又は受信用フィルタのバランス特性の劣化による感度劣化を抑えることができ、高性能な移動体通信機器を実現することができる。

【０１３５】以下に、図２１を参照しながら、上記平衡型高周波回路を有する通信機器の構成及び動作について説明する。ここで、図２１は、本発明の平衡型デバイスを用いた平衡型高周波回路２７０１のブロック図である。

【０１３６】図２１において、送信回路２７１１から出力される送信信号は、送信増幅器２７０２，送信フィルタ２７０３、スイッチ２７０４を介してアンテナ２７０５より送信される。

【０１３７】又、アンテナ２７０５より受信された受信信号は、スイッチ２７０４、受信フィルタ２７０６，受信増幅器２７０７を介して受信回路２７１２に入力される。

【０１３８】ここで、送信増幅器２７０２は平衡型であり、スイッチ２７０４は不平衡型であるので、送信フィルタ２７０３は不平衡－平衡型入出力端子を有する構成となる。又、受信増幅器２７０７は平衡型であり、スイッチ２７０４は不平衡型であるので、受信フィルタ２７０６は不平衡－平衡型入出力端子を有する構成となる。

【０１３９】本発明の弾性表面波フィルタを送信フィルタ２７０３，及び／又は受信フィルタ２７０６に適用することにより、バランス特性の劣化による送信時の変調精度の劣化を抑えることが出来る。又、バランス特性の劣化による受信時の感度劣化を抑えることが出来、高性能な平衡型高周波回路を実現することが出来る。

【０１４０】又、送信フィルタ２７０３と送信増幅器２７０２、あるいは受信フィルタ２７０６と受信増幅器２７０７を上述したモジュール構成としてもかまわない。

【０１４１】又、スイッチ素子と受信フィルタ、あるいは、スイッチ素子と送信フィルタを上述したモジュール構成としてもよい。

【０１４２】

【発明の効果】以上述べたことから明らかなように、本発明はバランス特性が良好であるという長所を有する。

【図面の簡単な説明】

【図１】（ａ）：本発明の実施の形態１における弾性表面波フィルタ素子の構成の模式図

（ｂ）：本発明の実施の形態１における回路基板の表層図

【図２】本発明の実施の形態１における配線電極と、回路基板上の回路基板上配線電極の配置関係を模式的に示す側面図

【図３】（ａ）：本発明の実施の形態１における他の弾性表面波フィルタ素子の構成を示す模式図

（ｂ）：本発明の実施の形態１における他の回路基板の表層図

【図４】本発明の実施の形態２における弾性表面波フィルタの構成を示す模式図

【図５】（ａ）：本発明の実施の形態２における弾性表面波フィルタ素子の構成を示す模式図

（ｂ）：本発明の実施の形態２における回路基板の表層図

【図６】本発明の実施の形態２におけるＩＤＴ電極と、回路基板上の回路基板上配線電極の配置関係を模式的に示す側面図

【図７】従来の弾性表面波フィルタを模式的に示した構成図

【図８】（ａ）：従来の弾性表面波フィルタ素子の構成模式図

（ｂ）：従来の回路基板の表層図

【図９】図８（ａ）におけるＡ－Ａ’での断面図

【図１０】寄生成分を考慮した場合の弾性表面波フィルタの構成の模式図

【図１１】（ａ）：弾性表面波フィルタの振幅を示す図

（ｂ）：位相バランス特性を示す図

【図１２】本発明の実施の形態１の弾性表面波フィルタの分解斜視図

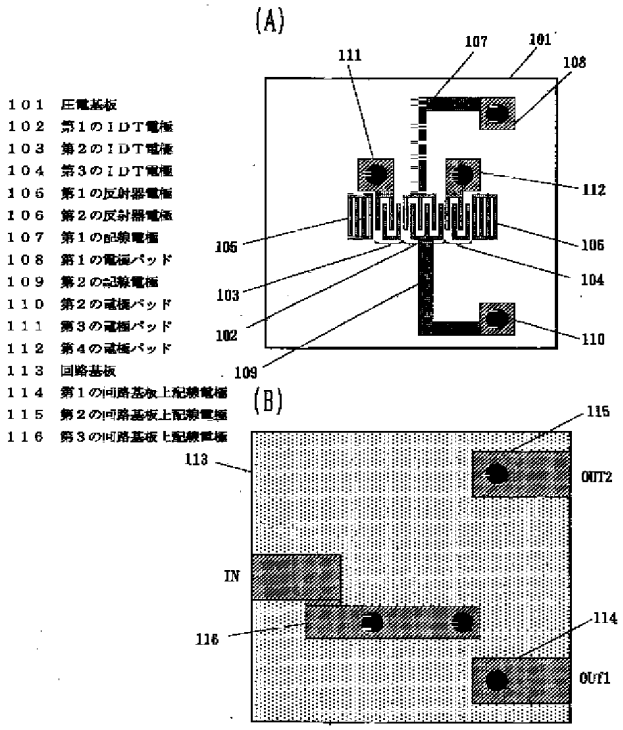
【図１３】本発明の実施の形態の変形例としての弾性表面波フィルタの分解斜視図

【図１４】図１３の構成例を模式的に表した図

【図１５】（ａ）：図３（ａ）に示した本発明の一実施の形態の弾性表面波フィルタ素子の変形例の構成を示す

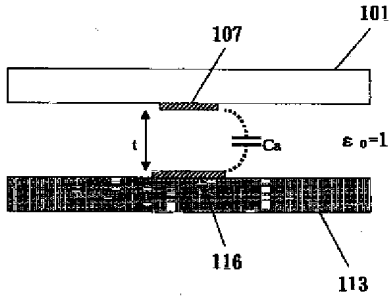
模式図
（ｂ）：図１５（ａ）に示す変形例に対応する回路基板の表層図
【図１６】本発明の弾性表面波フィルタの他の例としてのパッケージタイプの構成を示す模式図
【図１７】本発明のパッケージタイプ弾性表面波フィルタの他の構成を示す模式図
【図１８】（ａ）：本発明の弾性表面波フィルタ素子の他の例の模式図
（ｂ）：図１８（ａ）の弾性表面波フィルタ素子に対応する回路基板の表層図
【図１９】（ａ）：本発明の弾性表面波フィルタ素子の他の例の模式図
（ｂ）：図１９（ａ）の弾性表面波フィルタ素子のＡ－Ａ’断面図
（ｃ）：図１９（ａ）の弾性表面波フィルタ素子のＢ－Ｂ’断面図
【図２０】（ａ）：本発明のモジュールの一構成例を示す模式図
（ｂ）：図２０（ａ）を側面から見た模式図
【図２１】本発明の弾性表面波フィルタの通信機器への適用例を説明する構成図
【符号の説明】
１０１　圧電基板
１０２　第１のＩＤＴ電極
１０３　第２のＩＤＴ電極
１０４　第３のＩＤＴ電極
１０５　第１の反射器電極
１０６　第２の反射器電極
１０７　第１の配線電極
１０８　第１の電極パッド
１０９　第２の配線電極
１１０　第２の電極パッド
１１１　第３の電極パッド
１１２　第４の電極パッド
１１３　回路基板
１１４　第１の回路基板上配線電極
１１５　第２の回路基板上配線電極
１１６　第３の回路基板上配線電極
３０１　配線電極
３０２　電極パッド
３０３　第１の回路基板上配線電極
３０４　第２の回路基板上配線電極
３０５　第３の回路基板上配線電極
４０１　圧電基板
４０２　第１のＩＤＴ電極
４０３　第２のＩＤＴ電極
４０４　第３のＩＤＴ電極
４０５　第１の反射器電極
４０６　第２の反射器電極
４０７　平衡型端子の一方
４０８　平衡型端子の他方
４０９　不平衡型端子
４１０　弾性表面波共振子
５０１　第１の配線電極
５０２　第１の電極パッド
５０３　第２の配線電極
５０４　第２の電極パッド
５０５　第３の電極パッド
５０６　第４の電極パッド
５０７　第５の電極パッド
５０８　第６の電極パッド
５０９　回路基板
５１０　第１の回路基板上配線電極
５１１　第２の回路基板上配線電極
５１２　第３の回路基板上配線電極
５１３　第４の回路基板上配線電極
６０１　ＩＤＴ電極
６０２　回路基板上の配線電極
６０３　回路基板上の配線電極
６０４　寄生成分
７０１　圧電基板
７０２　第１のＩＤＴ電極
７０３　第２のＩＤＴ電極
７０４　第３のＩＤＴ電極
７０５　第１の反射器電極
７０６　第２の反射器電極
７０７　平衡型端子の一方
７０８　平衡型端子の他方
７０９　不平衡型端子
８０１　第１の配線電極
８０２　第１の電極パッド
８０３　第２の配線電極
８０４　第２の電極パッド
８０５　第３の配線電極
８０６　第３の電極パッド
８０７　回路基板
８０８　第１の回路基板上配線電極
８０９　第２の回路基板上配線電極
８１０　第３の回路基板上配線電極
１００１　容量成分

【図１】

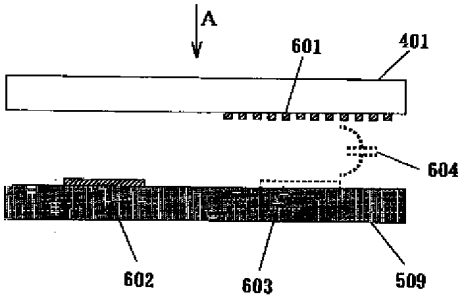


１０１　圧電基板
１０２　第１のＩＤＴ電極
１０３　第２のＩＤＴ電極
１０４　第３のＩＤＴ電極
１０５　第１の反射器電極
１０６　第２の反射器電極
１０７　第１の配線電極
１０８　第１の電極パッド
１０９　第２の配線電極
１１０　第２の電極パッド
１１１　第３の電極パッド
１１２　第４の電極パッド
１１３　回路基板
１１４　第１の回路基板上配線電極
１１５　第２の回路基板上配線電極
１１６　第３の回路基板上配線電極

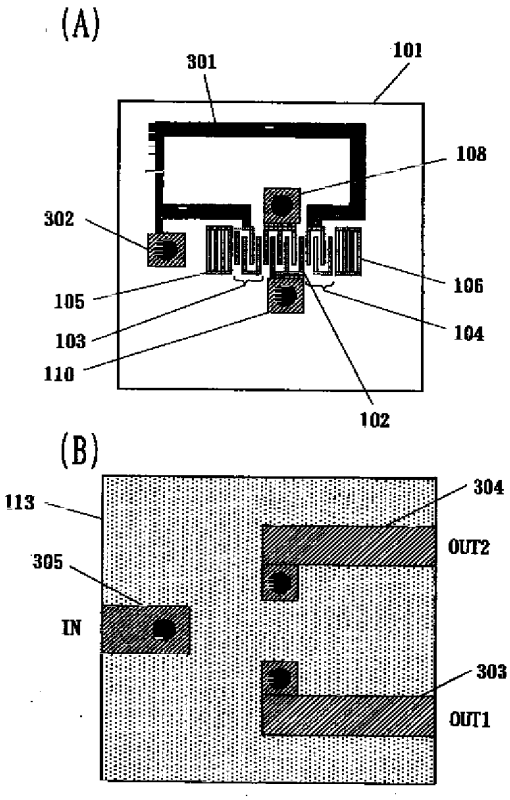
【図２】



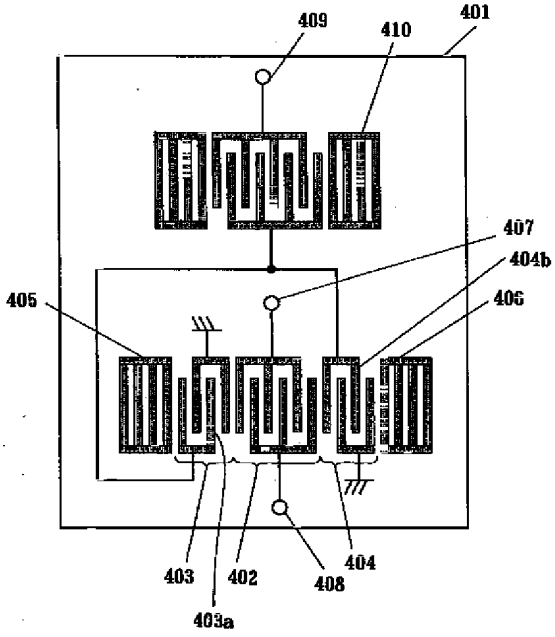
【図６】



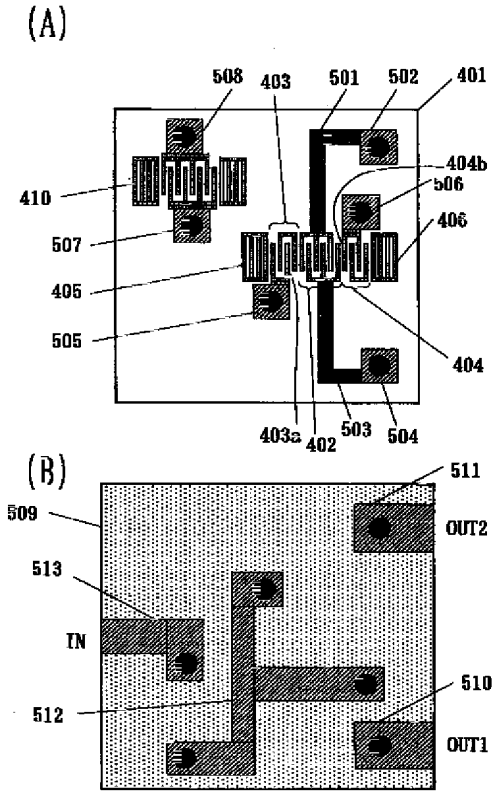
【図３】



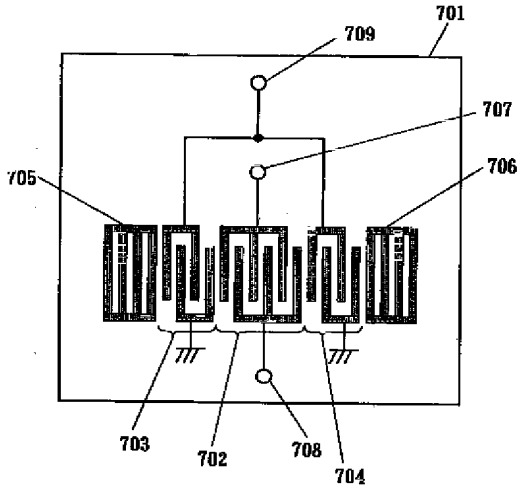
【図４】



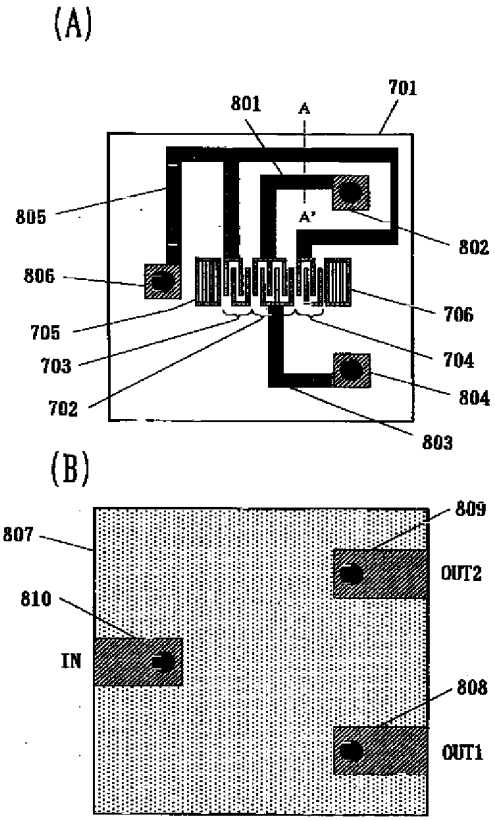
【図5】


(A)
508
403
501
502
401
410
404b
506
406
507
405
505
404
403a
402
503
504
(B)
511
509
OUT2
513
IN
510
512
OUT1

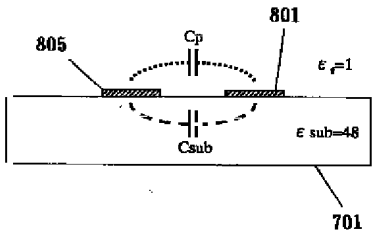
【図7】


701
709
707
705
706
703
702
708
704

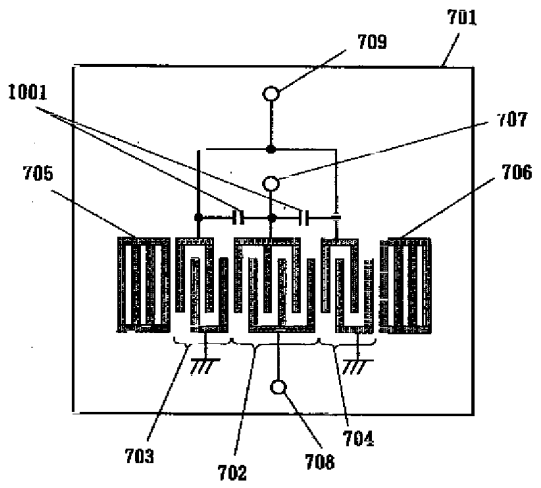
【図8】


(A)
801
A
701
805
A'
802
806
706
705
704
703
804
702
803
(B)
809
807
OUT2
810
IN
808
OUT1

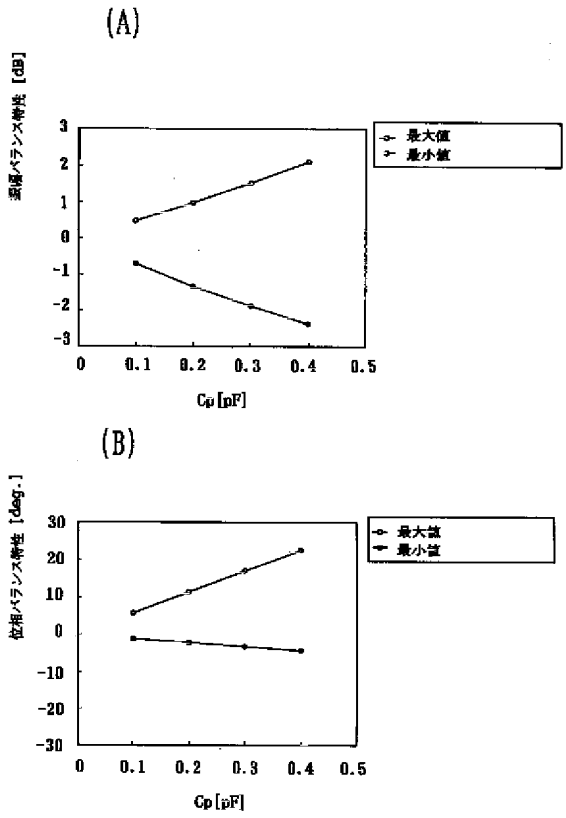
【図9】


805
Cp
801
ε r=1
ε sub=48
Csub
701

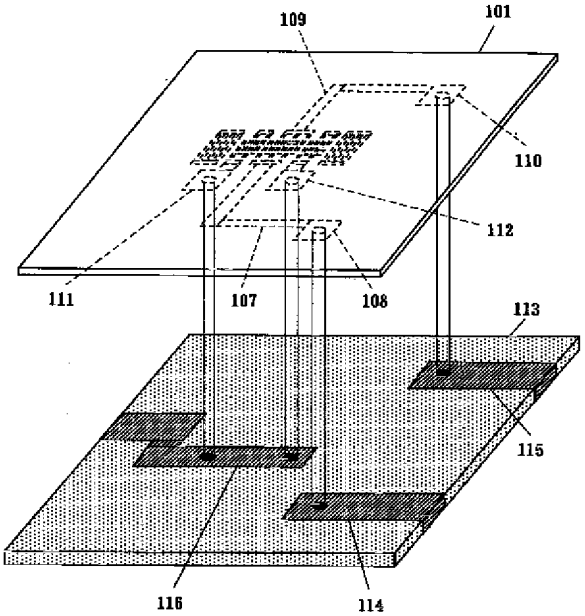
【図１０】



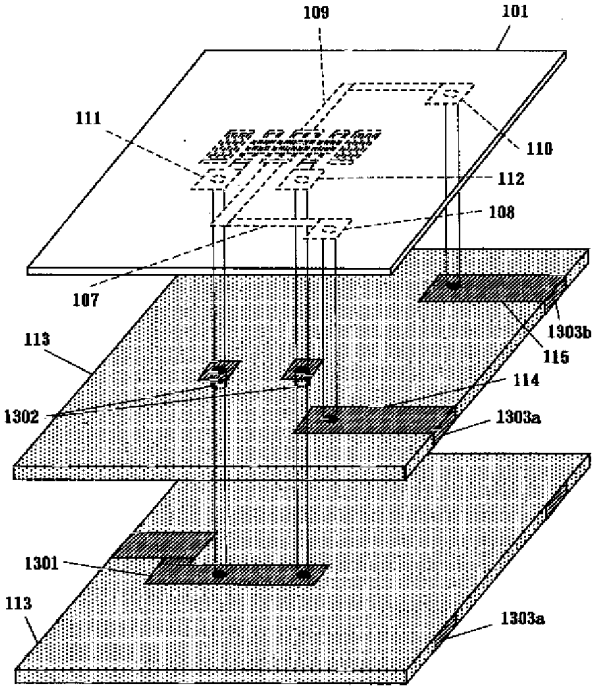
【図１１】



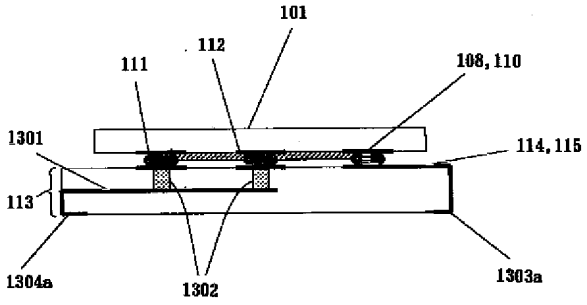
【図１２】



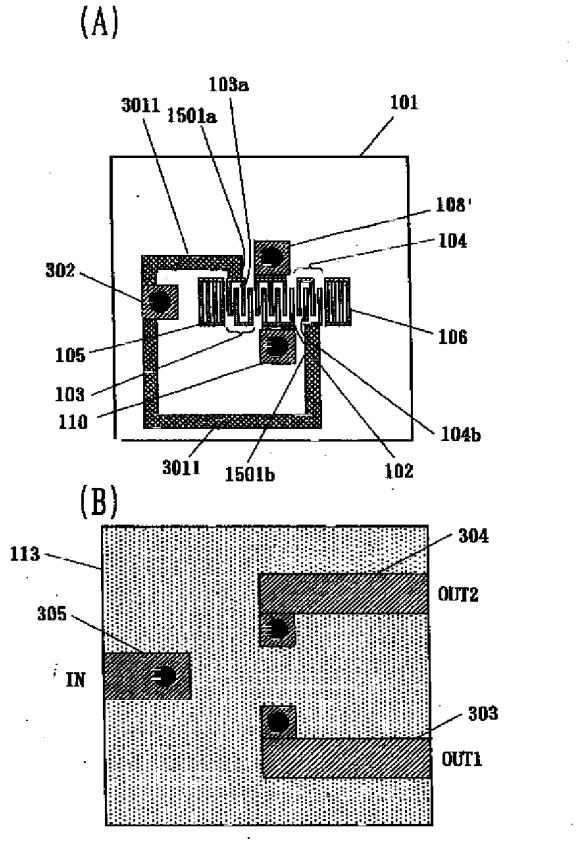
【図１３】



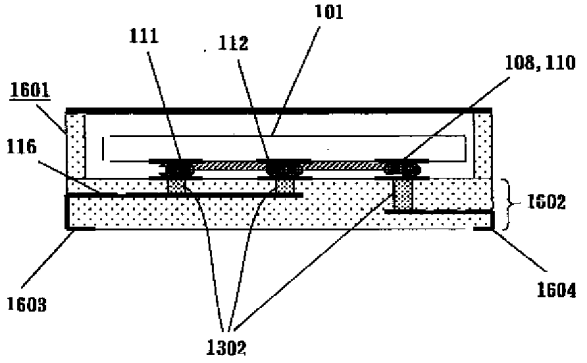
【図14】



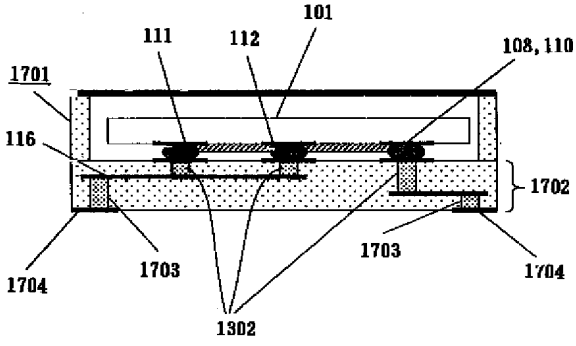
【図15】



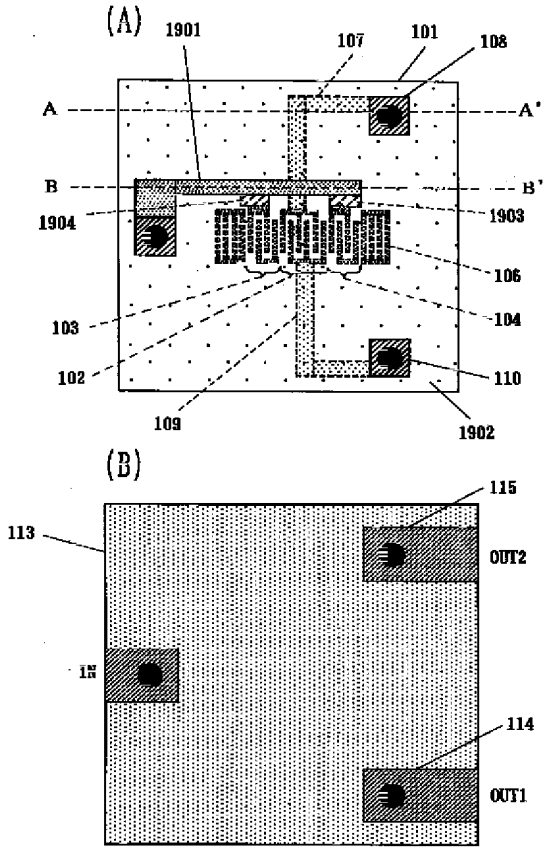
【図16】



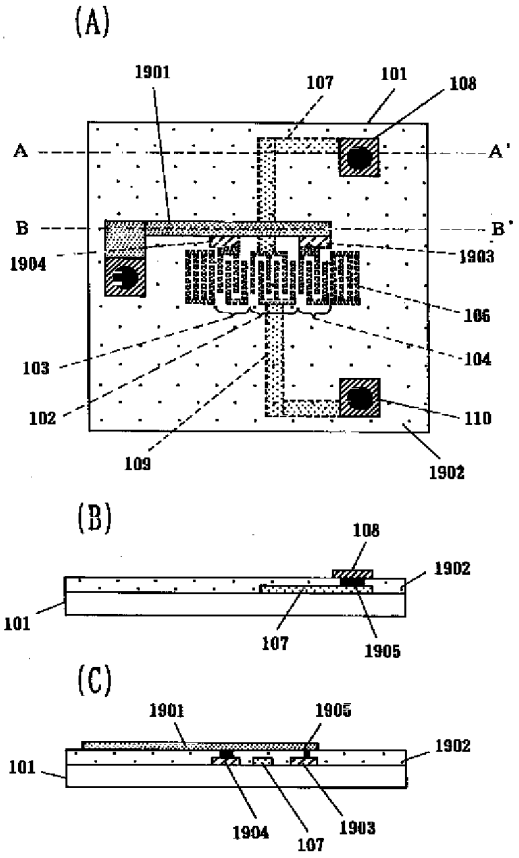
【図17】



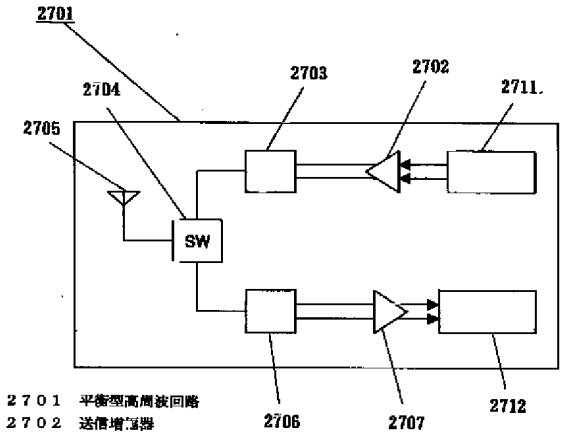
【図18】



【図19】

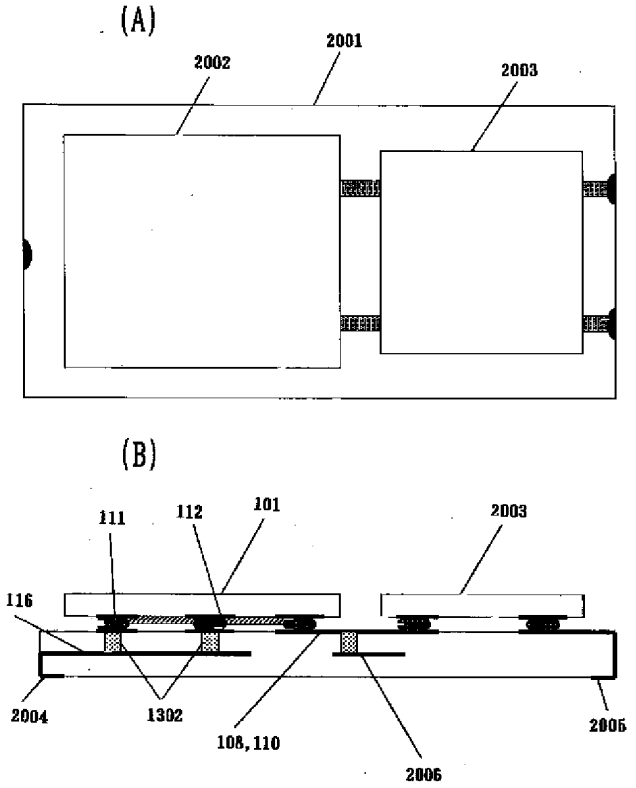


【図21】



2701 平衡型高周波回路
2702 送信増幅器
2703 送信フィルタ
2704 スイッチ
2705 アンテナ
2706 受信フィルタ
2707 受信増幅器
2711 送信回路
2712 受信回路

【図２０】



フロントページの続き

(72)発明者　常川　昭雄
大阪府門真市大字門真1006番地　松下電器産業株式会社内

(72)発明者　都築　茂
大阪府門真市大字門真1006番地　松下電器産業株式会社内

Ｆターム(参考)　5J097 AA11 AA29 BB14 CC04 FF05
GG03 GG04 HA04 JJ01 JJ09
KK10 LL06 LL08

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2003-204243

(43)Date of publication of application : 18.07.2003

(51)Int.Cl. H03H 9/25

H03H 9/145

(21)Application number : 2002-311730

(22)Date of filing : 25.10.2002

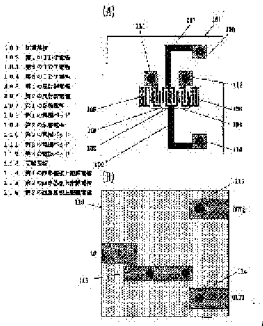
(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD

(72)Inventor : NAKAMURA HIROYUKI
ONISHI KEIJI
TSUNEKAWA AKIO
TSUZUKI SHIGERU

(30)Priority

Priority number : 2001330435 Priority date : 29.10.2001 Priority country : JP

(54) SURFACE ACOUSTIC WAVE FILTER ELEMENT, SURFACE ACOUSTIC WAVE FILTER, AND COMMUNICATION DEVICE USING THE SAME



(57)Abstract:

PROBLEM TO BE SOLVED: To solve the problem that balance characteristics are deteriorated in a surface acoustic wave (SAW) filter having a balanced terminal.

SOLUTION: One electrode finger of a first IDT electrode 102 is connected via a first wiring electrode 107 to a first electrode pad 108. The other electrode finger of the first IDT electrode 102 is connected via a second wiring electrode 109 to a second electrode pad 110. Electrode fingers on one side in second and third IDT electrodes 103 and 104 are substantially directly connected to third and fourth electrode pads 111 and 112.

LEGAL STATUS

[Date of request for examination] 21.10.2005

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's

decision of rejection]

[Date of requesting appeal against
examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

CLAIMS

[Claim(s)]

[Claim 1] It is the surface acoustic wave filter element equipped with a piezo-electric substrate and two or more INTADIJITARU transducer electrodes (IDT electrode) formed on said piezo-electric substrate. At least one IDT electrode is connected to a balanced type terminal among said two or more IDT electrodes. The 1st [which other IDT electrodes should be connected to a balanced type terminal or an unbalance mold terminal, and should be connected to said at least one IDT electrode] wiring electrode means by which **** connection was made, The surface acoustic wave filter element arranged on the flat surface where the 2nd [which should be connected to an IDT electrode besides the above] wiring electrode means by which **** connection was made differ mutually.

[Claim 2] It is the surface acoustic wave filter element according to claim 1 by which said other wiring electrode means are arranged on the circuit board in which said piezo-electric substrate should be mounted by arranging said one wiring electrode means on the principal plane of said piezo-electric substrate

among said 1st and 2nd wiring electrode means.

[Claim 3] (1) Said one wiring electrode means is formed on said piezo-electric substrate among said 1st and 2nd wiring electrode means. And said wiring electrode means of another side is the inner layer electrode of the circuit board with which said piezo-electric substrate should be mounted. (2) -- the surface acoustic wave filter element according to claim 1 said whose wiring electrode means of another side said one wiring electrode means is formed among said 1st and 2nd wiring electrode means on the circuit board in which said piezo-electric substrate should be mounted, and is the inner layer electrode of said circuit board. [or]

[Claim 4] The surface acoustic wave filter element according to claim 1 by which said one wiring electrode means is established on the principal plane of a piezo-electric substrate among said 1st and 2nd wiring electrode means, and said wiring electrode means of another side is established on the protective coat formed on said principal plane of said piezo-electric substrate.

[Claim 5] The surface acoustic wave filter element according to claim 4 said whose protective coat is a dielectric thin film.

[Claim 6] The surface acoustic wave filter element according to claim 1 which said surface acoustic wave filter element is a surface acoustic wave filter element of the longitudinal-mode mold which has arranged the 1st, 2nd, and 3rd IDT electrode and at least two reflector electrodes along the propagation direction of a surface acoustic wave, and is the configuration that the said 2nd and 3rd IDT electrode is arranged at the both sides of said 1st IDT electrode.

[Claim 7] The 1st and 2nd electrode pads prepared on said piezo-electric substrate, and the 3rd electrode pad which was prepared on said piezo-electric substrate and which was connected to said 2nd IDT electrode directly [parenchyma top], the 4th electrode pad which was prepared on said piezo-electric substrate and which was connected to said 3rd IDT electrode directly [parenchyma top] -- having -- (1) -- said 1st wiring electrode means means it prepares on said piezo-electric substrate as a wiring electrode of a pair -- having

-- **** -- (2) -- said 1st IDT electrode [and] It is a balanced type and, moreover, connects with the said 1st and 2nd electrode pad through each wiring electrode of the wiring electrode of said pair. Said 2nd wiring electrode means The surface acoustic wave filter element according to claim 6 by which the said 3rd and 4th electrode pad is connected to said 2nd wiring electrode means by being prepared in said circuit board and mounting said surface acoustic wave filter element in said circuit board.

[Claim 8] The 1st and the 2nd electrode pad which were prepared on said piezo-electric substrate and which were connected to said 1st IDT electrode directly [parenchyma top], the 3rd electrode pad prepared on said piezo-electric substrate -- having -- (1) -- said 2nd wiring electrode means Said 2nd and 3rd IDT electrodes are unbalance molds. it prepares on said piezo-electric substrate -- having -- **** -- (2) -- [and] It connects with said 3rd electrode pad through said 2nd wiring electrode means. And said 1st wiring electrode means The surface acoustic wave filter element according to claim 6 by which the said 1st and 2nd electrode pad is connected to said 1st wiring electrode means by being prepared in said circuit board and mounting said surface acoustic wave filter element in said circuit board.

[Claim 9] The surface acoustic wave filter element according to claim 7 which said 3rd electrode pad is connected to one electrode finger of said 2nd IDT electrode, and said 4th electrode pad is connected to the electrode finger of another side of said 3rd IDT electrode, and the electrode finger of said another side sees from one [said] electrode finger, and is prepared in the reverse side.

[Claim 10] The surface acoustic wave filter element according to claim 8 which it connects with one electrode finger of said 2nd IDT electrode, and said 2nd wiring electrode means is connected to the electrode finger of another side of said 3rd IDT electrode, and the electrode finger of said another side sees from one [said] electrode finger, and is prepared in the reverse side.

[Claim 11] Said surface acoustic wave filter element is a surface acoustic wave filter element according to claim 1 which is the configuration of having connected

to the ladder mold or the symmetry skeleton pattern the surface acoustic wave resonator constituted with the 1st IDT electrode and two reflector electrodes arranged at the both sides.

[Claim 12] The surface acoustic wave filter equipped with the circuit board in which the surface acoustic wave filter element and said surface acoustic wave filter element of any of claims 1-11 or one publication were mounted.

[Claim 13] The surface acoustic wave filter according to claim 12 with which said circuit board constitutes some ceramic packages.

[Claim 14] It is the surface acoustic wave filter according to claim 12 with which said circuit board is the layered product constituted with the dielectric, said surface acoustic wave filter element is a configuration mounted on said layered product, and said wiring electrode means is formed in said layered product maximum top face or said layered product inner layer.

[Claim 15] The surface acoustic wave filter according to claim 12 with which said IDT electrode and the wiring electrode means formed on said circuit board do not lap spatially and which is arranged like.

[Claim 16] The surface acoustic wave filter according to claim 12 said whose mounting is face down mounting.

[Claim 17] It is the surface acoustic wave filter element according to claim 1 characterized by being free space between said different flat surfaces.

[Claim 18] The surface acoustic wave filter element according to claim 1 with which it is satisfied of epsilonxS/t <=1.1x10-2 when area for an intersection of t, said 1st wiring electrode means, and said 2nd wiring electrode means is set to S for the distance between the said 1st [which is formed in epsilon and said different flat surface in the specific inductive capacity between said different flat surfaces, respectively], and 2nd wiring electrode means.

[Claim 19] Said piezo-electric substrate is a surface acoustic wave filter element according to claim 1 characterized by effective specific inductive capacity being 40 or more substrates.

[Claim 20] The surface acoustic wave filter element according to claim 19 as

which the ingredient of said piezo-electric substrate is chosen from lithium tantalate and lithium niobate.

[Claim 21] The surface acoustic wave filter element according to claim 1 characterized by being constituted so that the value of the admittance as a parasitism component of said 1st wiring electrode means and said 2nd wiring electrode means may be set to 0.6 or less mSs.

[Claim 22] The module equipped with the substrate with which claims 1-11, the surface acoustic wave filter element of any of 17-21 or one publication, the predetermined semiconductor device, and said surface acoustic wave filter element and said semiconductor device were mounted.

[Claim 23] Said substrate is a module according to claim 22 whose dielectric layer is the layered product by which the laminating was carried out.

[Claim 24] The module according to claim 22 said whose semiconductor device is a low noise amplifier.

[Claim 25] The module according to claim 24 said whose low noise amplifier is a balanced type.

[Claim 26] or [that said semiconductor device is a switching device] -- or the module according to claim 24 which is a mixer.

[Claim 27] (1) a piezo-electric substrate and (2) -- with the surface acoustic wave filter element which has two or more INTADIJITARU transducer electrodes (IDT electrode) formed on said piezo-electric substrate The 1st wiring electrode means for connecting at least one IDT electrode to the balanced type terminal in which it was prepared by said circuit board the circuit board in which said surface acoustic wave filter element was mounted, and among said two or more IDT electrodes, It has the 2nd wiring electrode means for connecting other IDT electrodes to the balanced type terminal or unbalance mold terminal in which it was prepared by said circuit board among said two or more IDT electrodes. Said 1st wiring electrode means, The surface acoustic wave filter arranged on the flat surface where said 2nd wiring electrode means differ mutually.

[Claim 28] the communication equipment equipped with an antenna, the

switching means connected to said antenna, said switching means, the transmitting filter prepared between sending circuits, and said switching means and the receiving filter prepared between receiving circuits -- it is -- said transmitting filter and/or said receiving filter -- claims 1-11 and 17- the communication equipment which has the surface acoustic wave filter element of any of 21 and 27, or one publication.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the surface acoustic wave filter element which has the balanced type terminal which suppressed degradation of electrical characteristics, a surface acoustic wave filter, a module, and communication equipment.
[0002]
[Description of the Prior Art] In recent years, high-performance-izing of the components used and a miniaturization are expected with development of mobile communications. Furthermore, equilibration of semi-conductor components, such

as IC, progresses for the purpose of good-izing of the property for a noise, and equilibration is called for also in the surface acoustic wave filter element used for RF stage.

[0003] Conventionally, as a filter of RF stages, such as mobile communication equipment, the surface acoustic wave filter is used widely. Balanced - unbalance conversion can realize easily especially the surface acoustic wave filter element of a longitudinal-mode mold.

[0004] Furthermore, the face down mounting technology represented by a flip chip, CSP (Chip Size Package), etc. is becoming in use from the conventional wire-bonding mounting technology about a miniaturization.

[0005] Hereafter, the surface acoustic wave filter element of the longitudinal-mode mold which has the conventional balanced blocking output terminal is explained.

[0006] The configuration of the surface acoustic wave filter of the longitudinal-mode mold which has the conventional balanced type terminal in drawing 7 is shown.

[0007] In drawing 7 , a surface acoustic wave filter element is constituted by the 1st, 2nd, and 3rd INTADIJITARU transducer electrode (an IDT electrode is called hereafter) 702, 703, and 704 and the 1st and 2nd reflector electrode 705 and 706 on the piezo-electric substrate 701. One electrode finger of the 1st IDT electrode 702 is connected to one side 707 of a balanced type terminal, and the electrode finger of another side of the 1st IDT electrode 702 is connected to another side 708 of a balanced type terminal.

[0008] Moreover, one near electrode finger of the 2nd and 3rd IDT electrode 703 and 704 is connected to the unbalance mold terminal 709, and another side is grounded. The surface acoustic wave filter element which has an unbalance mold-balanced type terminal is obtained by considering as the above configuration.

[0009] Next, an example about the configuration in the case of carrying out face down mounting of said surface acoustic wave filter element on the circuit board is

described. Drawing 8 (a) is drawing having shown typically the configuration on the piezo-electric substrate of the surface acoustic wave filter element of drawing 7 .

[0010] One electrode finger of the 1st IDT electrode 702 is connected to the 1st electrode pad 802 through the 1st wiring electrode 801. The electrode finger of another side of the 1st IDT electrode 702 is connected to the 2nd electrode pad 804 through the 2nd wiring electrode 803.

[0011] One near electrode finger of the 2nd IDT electrode 703 and one near electrode finger of the 3rd IDT electrode 704 are connected to the 3rd electrode pad 806 through the 3rd wiring electrode 805, respectively. Moreover, it is omitting about an earth electrode.

[0012] What is shown in drawing 8 (b) is a surface Fig. of the circuit board where the above-mentioned surface acoustic wave filter element is mounted. The 1st wiring-on the circuit board electrode 808, the 2nd wiring-on the circuit board electrode 809, and the 3rd wiring-on the circuit board electrode 810 are formed in the circuit board 807, respectively.

[0013] The surface acoustic wave filter element shown in drawing 8 (a) is mounted so that the circuit board 807 may be countered. For example, the mounting approach by the ultrasonic thermocompression bonding using a golden bump can be used. At this time, the 1st electrode pad 802 is connected to the 1st wiring-on the circuit board electrode 808, the 2nd electrode pad 804 is connected to the 2nd wiring-on the circuit board electrode 809, and the 3rd electrode pad 806 is connected to the 3rd wiring-on the circuit board electrode 810.

[0014] The 1st, 2nd, and 3rd wiring-on the circuit board electrode 808, 809, and 810 is drawn out by the electrode of a through hole, a beer hall, or the exterior of the circuit board etc. as a terminal. In this case, as for the 1st, 2nd, and 3rd electrode 808, 809, and 810, the surface acoustic wave filter of a balanced type output terminal which is connected to OUT1, another side OUT2 of a balanced type output terminal, and the unbalance blocking force terminal IN on the other hand, and has an unbalance mold-balanced type terminal is realized,

respectively.

[0015] moreover, the conventional surface acoustic wave device -- at least one of the electrode pads for touch-down of a surface acoustic element, and the touch-down of the package for surface mounts -- business -- the communication for touch-down which connects at least one of the external connection terminals -- whenever [out of band oppression] is improved by preparing two or more conductors in the package inside for surface mounts (for example, patent reference 1 reference.).

[0016] Moreover, although it is indicated that the electrical coupling between both IDT(s) must be oppressed as much as possible since a common mode voltage will occur if the conventional surface acoustic wave device has association between an unbalance blocking force terminal and the terminal of a balanced type IDT, it is not indicated about the concrete configuration (for example, nonpatent literature 1 reference.).

[0017]

[Patent reference 1] JP,11-145772,A [nonpatent literature 1] A year Institute of Electronics, Information and Communication Engineers foundation and "boundary society convention lecture 2001 Collected-works" Institute of Electronics, Information and Communication Engineers, August 29, 2001, p283-284[0018]

[Problem(s) to be Solved by the Invention] However, in an above-mentioned surface acoustic wave filter element or an above-mentioned surface acoustic wave filter, the wiring electrode configuration on the piezo-electric substrate with which there were few detailed arguments on the cause of the degradation, and they took the balance property into consideration, and the structure of the circuit board were not clarified about the balance property which is one of the important electrical characteristics.

[0019] In this invention, in consideration of such an above-mentioned conventional technical problem, the cause of degradation of a balance property is clarified about the surface acoustic wave filter element which has a balanced

type terminal, or a surface acoustic wave filter, the improvement is made, and it aims at offering the surface acoustic wave filter element which has a good balance property, a surface acoustic wave filter, a module, and communication equipment.

[0020]

[Means for Solving the Problem] Two or more INTADIJITARU transducer electrodes with which the 1st this invention was formed on the piezo-electric substrate (for example, sign 101) and said piezo-electric substrate It is the surface acoustic wave filter element which it had. (An IDT electrode is called hereafter) (for example, sign 102,103,104) The inside of two or more of said IDT electrodes (for example, sign 102,103,104), At least one IDT electrode (for example, sign 102) is connected to a balanced type terminal. Other IDT electrodes (for example, sign 103,104) are connected to a balanced type terminal or an unbalance mold terminal. The 1st [which should be connected to said at least one IDT electrode (for example, sign 102)] wiring electrode means by which **** connection was made (for example, sign 107,109), The 2nd [which should be connected to an IDT electrode besides the above] wiring electrode means (for example, sign 116) by which **** connection was made is the surface acoustic wave filter element arranged on a mutually different flat surface.

[0021] As for the 2nd this invention, said one wiring electrode means is arranged on the principal plane of said piezo-electric substrate among said 1st and 2nd wiring electrode means, and said other wiring electrode means are the surface acoustic wave filter elements of the 1st this invention of the above arranged on the circuit board (for example, sign 113) in which said piezo-electric substrate should be mounted.

[0022] Said one wiring electrode means is formed on said piezo-electric substrate among said 1st and 2nd wiring electrode means. the 3rd this invention -- (1) -- And said wiring electrode means of another side is the inner layer electrode of the circuit board with which said piezo-electric substrate should be mounted. (2) -- said one wiring electrode means is formed among said 1st and

2nd wiring electrode means on the circuit board in which said piezo-electric substrate should be mounted, and said wiring electrode means of another side is the surface acoustic wave filter element of the 1st this invention of the above which is the inner layer electrode of said circuit board. [or]

[0023] The 4th this invention is the surface acoustic wave filter element of the 1st this invention of the above by which said one wiring electrode means is established on the principal plane of a piezo-electric substrate among said 1st and 2nd wiring electrode means, and said wiring electrode means of another side is established on the protective coat (for example, sign 1902) formed on said principal plane of said piezo-electric substrate.

[0024] The 5th this invention is the surface acoustic wave filter element of the 4th this invention of the above said whose protective coat is a dielectric thin film.

[0025] Said surface acoustic wave filter element the 6th this invention The 1st, the 2nd, the 3rd IDT electrode (For example, the sign 102,103,104) and at least two reflector electrodes (For example, sign 105,106) It is the surface acoustic wave filter element of the longitudinal-mode mold arranged along the propagation direction of a surface acoustic wave, and is the surface acoustic wave filter element of the 1st this invention of the above which is the configuration that the said 2nd and 3rd IDT electrode is arranged at the both sides of said 1st IDT electrode.

[0026] The 1st and the 2nd electrode pad (for example, sign 108,110 in drawing 1 (a)) with which the 7th this invention was prepared on said piezo-electric substrate, The 3rd electrode pad which was prepared on said piezo-electric substrate and which was connected to said 2nd IDT electrode directly [parenchyma top] (for example, sign 111 in drawing 1 (a)), The 4th electrode pad which was prepared on said piezo-electric substrate and which was connected to said 3rd IDT electrode directly [parenchyma top] (For example, sign 112 in drawing 1 (a)) having -- (1) -- said 1st wiring electrode means means it prepares on said piezo-electric substrate as a wiring electrode (for example, signs 107 and 109) of a pair -- having -- **** -- (2) -- said 1st IDT electrode (for

example, sign 102) [and] It is a balanced type and, moreover, each wiring electrode of the wiring electrode (for example, signs 107 and 109) of said pair is minded. Said 1st [the], the 2nd electrode pad It connects with (for example, the sign 108,110). Said 2nd wiring electrode means (for example, sign 116) By being prepared in said circuit board (for example, sign 113), and mounting said surface acoustic wave filter element in said circuit board The said 3rd and 4th electrode pad (for example, sign 111,112) is the surface acoustic wave filter element of the 6th this invention of the above connected to said 2nd wiring electrode means (for example, sign 116).

[0027] The 1st and the 2nd electrode pad (for example, sign 108,110 in drawing 3 (a)) with which the 8th this invention was prepared on said piezo-electric substrate and which were connected to said 1st IDT electrode directly [parenchyma top], The 3rd electrode pad prepared on said piezo-electric substrate (for example, sign 101) (For example, sign 302 in drawing 3 (a)) having -- (1) -- said 2nd wiring electrode means (for example, sign 301 in drawing 3 (a)) it prepares on said piezo-electric substrate -- having -- **** -- (2) -- said 2nd [the] and the 3rd an IDT electrode [and] Inner sign 103,104) is an unbalance mold. (-- for example, drawing 3 (a) -- Said 2nd wiring electrode means (for example, sign 301) is minded. And said 3rd electrode pad It connects with (for example, the sign 302). Said 1st wiring electrode means (for example, sign 303,304 in drawing 3 (b)) By being prepared in said circuit board (for example, sign 113 in drawing 3 (b)), and mounting said surface acoustic wave filter element in said circuit board The said 1st and 2nd electrode pad is the surface acoustic wave filter element of the 6th this invention of the above connected to said 1st wiring electrode means.

[0028] Said 3rd electrode pad (for example, sign 505 in drawing 5 (a)) the 9th this invention Said 2nd IDT electrode It connects with one electrode finger (for example, sign 403a in drawing 5 (a)) of inner 403). (-- for example, drawing 5 (a) -- Said 4th electrode pad (for example, sign 506 in drawing 5 (a)) And said 3rd IDT electrode (-- for example, drawing 5 (a) -- it is the surface acoustic wave filter element of the 7th this invention of the above which it connects with the electrode

finger of another side of inner sign 404), and the electrode finger of said another side sees from one [said] electrode finger, and is prepared in the reverse side.

[0029] The 10th this invention said 2nd wiring electrode means (for example, sign 3011 in drawing 15 (a)) One electrode finger of said 2nd IDT electrode (for example, sign 103 in drawing 15 (a)) It connects with inner sign 103a). (-- for example, drawing 15 (a) -- The electrode finger of another side of said 3rd IDT electrode (for example, sign 104 in drawing 15 (a)) It connects with inner sign 104a). (-- for example, drawing 15 (a) -- said another side an electrode finger (-- for example, drawing 15 (a) -- inner sign 104b) is the surface acoustic wave filter element of the 8th this invention of the above which sees from one [said] electrode finger (for example, sign 103a in drawing 15 (a)), and is prepared in the reverse side.

[0030] The 11th this invention is the surface acoustic wave filter element of the 1st this invention of the above which is the configuration of having connected to the ladder mold or the symmetry skeleton pattern the surface acoustic wave resonator which said surface acoustic wave filter element consists of with the 1st IDT electrode and two reflector electrodes arranged at the both sides.

[0031] The 12th this invention is the surface acoustic wave filter equipped with the circuit board in which the surface acoustic wave filter element and said surface acoustic wave filter element of any one this invention of the above 1-11ths were mounted.

[0032] The 13th this invention is a surface acoustic wave filter of the 12th this invention of the above with which said circuit board constitutes some ceramic packages.

[0033] The 14th this invention is the layered product which said circuit board consisted of with the dielectric, said surface acoustic wave filter element is a configuration mounted on said layered product, and said wiring electrode means is the surface acoustic wave filter of the 12th this invention of the above prepared in said layered product maximum top face or said layered product inner layer.

[0034] The 15th this invention is a surface acoustic wave filter of the 12th this

invention of the above arranged like with which said IDT electrode and the wiring electrode means formed on said circuit board do not lap spatially.

[0035] The 16th this invention is the surface acoustic wave filter of the 12th this invention of the above said whose mounting is face down mounting.

[0036] The 17th this invention is the surface acoustic wave filter element of the 1st this invention of the above characterized by being free space between said different flat surfaces.

[0037] The 18th this invention is the surface acoustic wave filter element of the 1st this invention of the above with which are satisfied of epsilonxS/t <=1.1x10-2, when area for an intersection of t, said 1st wiring electrode means, and said 2nd wiring electrode means is set to S for the distance between the said 1st [which is formed in epsilon and said different flat surface in the specific inductive capacity between said different flat surfaces, respectively], and 2nd wiring electrode means.

[0038] The 19th this invention is the surface acoustic wave filter element of the 1st this invention of the above to which, as for said piezo-electric substrate, effective specific inductive capacity is characterized by being 40 or more substrates.

[0039] The 20th this invention is the surface acoustic wave filter element of the 19th this invention of the above as which the ingredient of said piezo-electric substrate is chosen from lithium tantalate and lithium niobate.

[0040] The 21st this invention is the surface acoustic wave filter element of the 1st this invention of the above characterized by being constituted so that the value of the admittance as a parasitism component of said 1st wiring electrode means and said 2nd wiring electrode means may be set to 0.6 or less mSs.

[0041] The 22nd this invention is the module equipped with the substrate with which the surface acoustic wave filter element, the predetermined semiconductor device, and said surface acoustic wave filter element and said semiconductor device of the above 1-11ths and any one this invention of 17-21 were mounted.

[0042] The 23rd this invention is the module of the 22nd publication of the above

said whose substrate is the layered product to which the laminating of the dielectric layer was carried out.

[0043] The 24th this invention is the module of the 22nd this invention of the above said whose semiconductor device is a low noise amplifier.

[0044] The 25th this invention is the module of the 24th this invention of the above said whose low noise amplifier is a balanced type.

[0045] or [that said semiconductor device of the 26th this invention is a switching device] -- or it is the module of the 24th this invention of the above which is a mixer.

[0046] the 27th this invention -- (1) piezo-electricity substrate and (2) -- with the surface acoustic wave filter element which has two or more INTADIJITARU transducer electrodes (IDT electrode) formed on said piezo-electric substrate The 1st wiring electrode means for connecting at least one IDT electrode to the balanced type terminal in which it was prepared by said circuit board the circuit board in which said surface acoustic wave filter element was mounted, and among said two or more IDT electrodes, It has the 2nd wiring electrode means for connecting other IDT electrodes to the balanced type terminal or unbalance mold terminal in which it was prepared by said circuit board among said two or more IDT electrodes. Said 1st wiring electrode means, Said 2nd wiring electrode means is the surface acoustic wave filter arranged on a mutually different flat surface.

[0047] the communication equipment with which the 28th this invention was equipped with an antenna, the switching means connected to said antenna, said switching means, the transmitting filter prepared between sending circuits, and said switching means and the receiving filter prepared between receiving circuits -- it is -- said transmitting filter and/or said receiving filter -- the above 1-11ths and 17- it is the communication equipment which has the surface acoustic wave filter element of any one this invention of 21 and 27.

[0048]

[Embodiment of the Invention] (Gestalt 1 of operation) It explains hereafter,

referring to a drawing about the surface acoustic wave filter element and surface acoustic wave filter of a gestalt 1 of operation of this invention.

[0049] First, consideration about the cause of degradation of the balance property of the above-mentioned surface acoustic wave filter element is performed. What is shown in drawing 9 is the sectional view cut down by A-A' in the surface acoustic wave filter of drawing 8 (a). Generally as for such a surface acoustic wave, piezo-electric substrates, such as a lithium acid tantalum (LiTaO3) and lithium acid niobium (LiNbO3), are used widely, and the effective specific inductive capacity of such a substrate is 48 or about 49, and a large value, respectively. Here, it is defined as effective specific inductive capacity using specific-inductive-capacity tensor epsilon11T of a piezo-electric substrate, and epsilon33T as the degree type 1.

[0050]

[Equation 1]

$$\sqrt{\{(\varepsilon_{11}{}^{T}) \times (\varepsilon_{33}{}^{T})\}}$$

As shown in drawing 9 , between the 1st wiring electrode 801 and the 3rd wiring electrode 805, the parasitism component Csub through a substrate, the spatial parasitism component Cp, etc. arise.

[0051] Since specific inductive capacity is large when wiring using a wiring electrode on a piezo-electric substrate, the effect also becomes large. Moreover, although association by the parasitism component can be small performed if the distance of these electrodes is detached, a surface acoustic wave filter element also needs to be miniaturized for coincidence in fact, and there is a limitation in enlarging distance of these electrodes.

[0052] The configuration which took these parasitism components into consideration to drawing 10 is shown. As a parasitism component in the surface acoustic wave filter of drawing 7 , the configuration which assumed the capacity component 1001 to I/O IDT inter-electrode can be considered. The capacity value of the capacity component 1001 is changed with the configuration shown in

drawing 10 , and the result of having analyzed about the filter of a 900MHz band is shown in drawing 11 (a) and drawing 11 (b).

[0053] Drawing 11 (a) and drawing 11 (b) are drawings having shown the amplitude balance property and the phase balance property as an index showing a balance property.

[0054] Here, the amplitude balance property is as follows. That is, the signal inputted from the unbalance mold terminal 709 of the surface acoustic wave filter element shown in drawing 7 or drawing 10 is outputted to 708 of one 707 and another side of a balanced type terminal as a balance signal. The thing showing the amplitude difference of the signal amplitude outputted to one 707 of the balanced type terminal in that case and the signal amplitude outputted to 708 of another side of a balanced type terminal is an amplitude balance property. And if this value serves as zero, it can be said that there is no degradation of a balance property.

[0055] Moreover, a phase balance property expresses the gap from 180 degrees of the phase contrast of the phase of the signal outputted to one 707 of the above-mentioned balanced type terminal and the phase of the signal outputted to 708 of another side of the above-mentioned balanced type terminal. And if this value serves as zero, it can be said that there is no degradation of a balance property.

[0056] Drawing 11 (a) and drawing 11 (b) show the maximum and the minimum value of the amplitude and the balance property of a phase in a passband. Drawing 11 (a) is an amplitude balance property, and drawing 11 (b) is a phase balance property.

[0057] The balance property has deteriorated, so that capacity value becomes large, as shown in drawing 11 (a) and drawing 11 (b). That is, a balance property deteriorates, so that association by the parasitism component during I/O is large.

[0058] In order to realize [an amplitude balance property] the filter of less than **10 degrees for less than **1dB and a phase balance property, it is necessary to set capacity value as a parasitism component during I/O to 0.10pF or less.

Namely, when it thinks of the admittance component Y, Y should just carry out from Y=2pifC to below 0.6 [mS]. f is a frequency and C is capacity value here.

[0059] Next, the configuration of the surface acoustic wave filter element which conquers the cause of degradation of the above-mentioned balance property, and a surface acoustic wave filter is described.

[0060] Drawing 1 (a) is drawing having shown typically the configuration on the piezo-electric substrate of a surface acoustic wave filter element. One electrode finger of the 1st IDT electrode 102 is connected to the 1st electrode pad 108 through the 1st wiring electrode 107.

[0061] The electrode finger of another side of the 1st IDT electrode 102 is connected to the 2nd electrode pad 110 through the 2nd wiring electrode 109.

[0062] One near electrode finger of the 2nd and 3rd IDT electrode 103 and 104 is connected to the 3rd and 4th electrode pad 111 and 112 directly [parenchyma top]. Although the near electrode finger of another side of the 2nd and 3rd IDT electrode 103 and 104 is grounded, it is omitted about an earth electrode here.

[0063] What is shown in drawing 1 (b) is a surface Fig. of the circuit board where the above-mentioned surface acoustic wave filter element is mounted. The 1st, 2nd, and 3rd wiring-on the circuit board electrode 114, 115, and 116 is formed in the circuit board 113.

[0064] The surface acoustic wave filter element shown in drawing 1 (a) is mounted so that the circuit board 113 may be countered (refer to drawing 12). Here, drawing 12 is the decomposition perspective view of the surface acoustic wave filter mounted so that a surface acoustic wave filter element might counter the circuit board 113.

[0065] For example, the mounting approach by the ultrasonic thermocompression bonding using a golden bump can be used.

[0066] At this time, the 1st electrode pad 108 is connected to the 1st wiring-on the circuit board electrode 114, the 2nd electrode pad 110 is connected to the 2nd wiring-on the circuit board electrode 115, and the 3rd and 4th electrode pad 111 and 112 is connected to two places of the 3rd wiring-on the circuit board

electrode 116.

[0067] At this time, the wiring electrode 116 on the circuit board bears a role of a wiring electrode for connecting electrically the same role 111 as the 3rd wiring electrode 805 of drawing 8 (a), i.e., the 3rd electrode pad, and the 4th electrode pad 112.

[0068] The 1st, 2nd, and 3rd wiring-on the circuit board electrode 114, 115, and 116 is drawn out by the electrode of a through hole, a beer hall, or the exterior of the circuit board etc. as a terminal.

[0069] In this case, as for the 1st, 2nd, and 3rd electrode 114, 115, and 116, the surface acoustic wave filter of a balanced type output terminal which is connected to OUT1, another side OUT2 of a balanced type output terminal, and the unbalance blocking force terminal IN on the other hand, and has an unbalance mold-balanced type terminal is realized, respectively.

[0070] By considering as the above configuration, the wiring electrode 116 on the 3rd circuit board connected to the 1st [in the 1st IDT electrode] and 2nd wiring electrode 107 and 109 and the 2nd and 3rd IDT electrode serves as arrangement left spatially.

[0071] According to such a configuration, compared with the configuration shown in drawing 8 (a), association during I/O can be suppressed clearly to the minimum, and the balance property of a surface acoustic wave filter element can be improved.

[0072] In addition, the 1st wiring electrode means of this invention corresponds to the wiring electrode of the pair expressed with the 1st of drawing 1 (a), and the 2nd wiring electrode 107,109. Moreover, the 2nd wiring electrode means of this invention corresponds to the 3rd wiring-on the circuit board electrode 116 shown in drawing 1 (b).

[0073] Moreover, in drawing 2 , although the crossing part produces the 1st wiring electrode 107 and the wiring electrode 116 on the 3rd circuit board, the parasitism component calcium in this part is expressed with the degree type 2, when a part for an intersection is assumed as an parallel plate capacitor in

approximation.

[0074]

[Equation 2] It becomes calcium=epsilon 0xS/t.

[0075] Here, epsilon 0 is the dielectric constant of free space, S is the area for an intersection and t is an inter-electrode distance.

[0076] For example, if S=100micrometerx100micrometer and t= 20 micrometers, calcium will serve as 4.4 [fF] and a small value from a formula 2.

[0077] In addition, although it is necessary to also take into consideration elements other than an intersection part in fact, and to optimize the configuration of a piezo-electric substrate and the circuit board, if it is the arrangement left spatially, association during I/O can be conventionally made small and the effectiveness that a balance property improves will be acquired similarly.

[0078] Moreover, since the height of the whole filter including a substrate becomes high a little in wiring by losing the wiring electrode on the piezo-electric substrate of a surface acoustic wave filter element, and using the circuit board as a multilayer substrate, when low back-ization is considered, it becomes a fault, but about a balance property, if it is the substrate of small specific inductive capacity, there is effectiveness of an improvement.

[0079] For example, the layered product which consists of an alumina or a ceramic dielectric as the circuit board is mentioned, and such specific inductive capacity has about ten thing. In this case, in a front type, calcium is set to 0.04 [pF] and understood that degradation of a balance property is smaller than drawing 11 .

[0080] Therefore, in order to consider as a configuration in which the multilayer interconnection within these circuit boards is carried out, and a parasitism component is set to 0.1pF or less, the specific inductive capacity epsilon of a circuit board ingredient, the wiring inter-electrode distance t, and relation with the area S for an intersection of a wiring electrode are [0081].

[Equation 3] It is desirable to fill epsilonxS/t <=1.1x10-2.

[0082] However, what is necessary is just to satisfy the above-mentioned relation

between [whole] flat surfaces, when the ingredient of specific inductive capacity with which plurality differs exists between flat surfaces.

[0083] Moreover, in the gestalt of this operation, the wiring electrodes 107 and 109 of the balancing side were formed on the piezo-electric substrate 101, and the unbalance side is connected with the wiring electrode 116 on the circuit board on the circuit board directly [parenchyma top]. However, as shown not only in this but in drawing 3 , the 2nd by the side of unbalance and the 3rd IDT electrode 103 and 104 are connected to the electrode pad 302 through the wiring electrode 301, and the 1st and 2nd electrode pad 108 and 110 is not cared about as a configuration connected to the 1st IDT electrode 102 directly [parenchyma top].

[0084] At this time, the 1st and 2nd electrode pad 108 and 110 is connected to the wiring electrodes 303 and 304 on the circuit board. Therefore, the wiring electrode 303 on the circuit board bears a role of the same wiring electrode as the 1st wiring electrode 801 of drawing 8 (a). Moreover, the wiring electrode 304 on the circuit board bears a role of the same wiring electrode as the 2nd wiring electrode 803 of drawing 8 (a).

[0085] Moreover, the 3rd electrode pad 302 is connected to the wiring electrode 305 on the circuit board. In this case, the wiring electrode 303,304,305 on the circuit board by which the surface of the circuit board 113 is arranged is suitably arranged according to the configuration of the surface acoustic wave on the piezo-electric substrate 101.

[0086] Also in the above configuration, the wiring electrode 303,304 on the 1st [in the 1st IDT electrode] and 2nd circuit board and the wiring electrode 301 of the 2nd and 3rd IDT electrode can serve as arrangement left spatially, can suppress association during I/O to the minimum, and can improve the balance property of a surface acoustic wave filter.

[0087] In addition, the 1st wiring electrode means of this invention corresponds to the 1st of drawing 3 (b), and the wiring electrode of the pair expressed by the 2nd wiring-on the circuit board electrode 303,304. Moreover, the 2nd wiring electrode

means of this invention corresponds to the wiring electrode 301 shown in drawing 3 (a).

[0088] In addition, in this operation gestalt, although explained as the circuit board, this may be a package etc.

[0089] Moreover, in the gestalt of this operation, although one near electrode finger of the 2nd and 3rd IDT electrode 103,104 explained the configuration connected to the 3rd and 4th electrode pad 111,112 directly [parenchyma top], you may connect for example, not only through this but through the bus bar electrode etc., and it should just be optimized with a configuration to which the die length of wiring becomes short.

[0090] (Gestalt 2 of operation) The surface acoustic wave filter element and surface acoustic wave filter of a gestalt 2 of operation of this invention are hereafter explained with reference to a drawing.

[0091] A surface acoustic wave filter element is constituted in drawing 4 by the surface acoustic wave resonator 410 constituted on the piezo-electric substrate 401 with the 1st, 2nd, and 3rd IDT electrode 402, 403, and 404, the 1st and 2nd reflector electrode 405 and 406, and an IDT electrode and a reflector electrode.

[0092] One electrode finger of the 1st IDT electrode 402 is connected to one side 407 of a balanced type terminal, and the electrode finger of another side of the 1st IDT electrode 402 is connected to another side 408 of a balanced type terminal.

[0093] Moreover, the unbalance mold terminal 409 is connected to one near electrode finger 403a of the 2nd IDT electrode 403, and electrode finger 404b of another side of the 3rd IDT electrode 404 through the surface acoustic wave resonator 410.

[0094] Here, as it is indicated in drawing 4 and drawing 5 as one near electrode finger 403a of the 2nd IDT electrode 403, and electrode finger 404b of another side of the 3rd IDT electrode 404, it is the electrode finger with which it sees from one side and another side is arranged at the reverse side.

[0095] The surface acoustic wave filter element which has an unbalance mold-

balanced type terminal is obtained by considering as the above configuration.

[0096] Next, an example about the configuration in the case of carrying out face down mounting of said surface acoustic wave filter element on a package or a substrate is described. Drawing 5 (a) is drawing having shown typically the configuration on the piezo-electric substrate of a surface acoustic wave filter element.

[0097] One electrode finger of the 1st IDT electrode 402 is connected to the 1st electrode pad 502 through the 1st wiring electrode 501. The electrode finger of another side of the 1st IDT electrode 402 is connected to the 2nd electrode pad 504 through the 2nd wiring electrode 503.

[0098] One near electrode finger of the 2nd IDT electrode 403 is connected to the 3rd electrode pad 505 directly [parenchyma top]. The near electrode finger of another side of the 3rd IDT electrode 404 is connected to the 4th electrode pad 506 directly [parenchyma top].

[0099] Although the near electrode finger of another side of the 2nd IDT electrode 403 and one near electrode finger of the 3rd IDT electrode 404 are grounded, the publication is omitted about an earth electrode here.

[0100] Furthermore, in one side and another side of an IDT electrode of the surface acoustic wave resonator 410, it connects with the 5th and 6th electrode pad 507 and 508 directly [parenchyma top].

[0101] What is shown in drawing 5 (b) is a surface Fig. of the circuit board where the above-mentioned surface acoustic wave filter element is mounted. The 1st, 2nd, 3rd, and 4th wiring-on the circuit board electrode 510, 511, 512, and 513 is formed in the circuit board 509.

[0102] The surface acoustic wave filter element shown in drawing 5 (a) is mounted so that the circuit board 509 may be countered.

[0103] For example, the mounting approach by the ultrasonic thermocompression bonding using a golden bump can be used. At this time, the 1st electrode pad 502 is connected to the 1st wiring-on the circuit board electrode 510, the 2nd electrode pad 504 is connected to the 2nd wiring-on the

circuit board electrode 511, and the 3rd and 4th electrode pad 505 and 506 is connected to the 3rd wiring-on the circuit board electrode 512.

[0104] Moreover, the 5th electrode pad 507 is connected to the 4th wiring-on the circuit board electrode 513, and the 6th electrode pad 508 is connected to the 3rd wiring-on the circuit board electrode 512.

[0105] That is, a role of the wiring electrode which three electrode pads are connected to the 3rd wiring-on the circuit board electrode 512, and connects the 2nd and 3rd IDT electrode 403 and 404 with the elastic wave resonator 410 is played.

[0106] Moreover, the 1st, 2nd, and 4th wiring-on the circuit board electrode 510, 511, and 513 is drawn out by the electrode of a through hole, a beer hall, or the exterior of the circuit board etc. as a terminal.

[0107] In this case, as for the 1st, 2nd, and 4th electrode 510, 511, and 513, the surface acoustic wave filter of a balanced type output terminal which is connected to OUT1, another side OUT2 of a balanced type output terminal, and the unbalance blocking force terminal IN on the other hand, and has an unbalance mold-balanced type terminal is realized, respectively.

[0108] By considering as the above configuration, the 3rd wiring-on the circuit board electrode 512 connected to the 1st [in the 1st IDT electrode] and 2nd wiring electrode 501 and 503 and the 2nd and 3rd IDT electrode can serve as arrangement left spatially, can suppress association during I/O to the minimum, and can improve the balance property of a surface acoustic wave filter element.

[0109] When the observation result of the filter of this invention and the filter of the conventional configuration was compared and the balance property was actually evaluated with the filter of a 1.8GHz band, the result by which the deflection (difference of maximum and the minimum value) of the amplitude and a phase balance property is improved about 25% was obtained by considering as the configuration of this invention.

[0110] Furthermore, a parasitism component can be further made small by considering as the configuration with which the wiring electrode on the circuit

board and the IDT electrode formed on a piezo-electric substrate do not lap spatially.

[0111] That is, when the piezo-electric substrate 401 is seen along the direction of the arrow head A shown in drawing 6 , as shown in drawing 6 , it is effective to consider as the configuration with which the IDT electrode 601 and the wiring electrode 602 on the circuit board do not lap. If the wiring electrode on the circuit board is prepared in the part 603 temporarily shown with the broken line of drawing 6 , the parasitism component 604 will arise between IDT electrodes, and it will become the cause of degradation of an electrical property.

[0112] In addition, the gestalt of the above-mentioned implementation described focusing on the example in which one of wiring electrodes is prepared on a piezo-electric substrate among the 1st of this invention, and the 2nd wiring electrode, and other wiring electrodes are prepared on the circuit board.

[0113] not only this but (1) -- among said 1st and 2nd wiring electrodes [however,] Said one wiring electrode is formed on said piezo-electric substrate, and the configuration which is the inner layer electrode of the circuit board with which said piezo-electric substrate should be mounted is sufficient as said wiring electrode of another side, and (refer to drawing 13) (2) -- said one wiring electrode may be formed among said 1st and 2nd wiring electrodes on the circuit board in which said piezo-electric substrate should be mounted, and the configuration (illustration abbreviation) which is the inner layer electrode of said circuit board is sufficient as said wiring electrode of another side. [or]

[0114] Here, drawing 13 is the decomposition perspective view of the former example of a configuration, and, unlike the case of drawing 12 , the wiring electrode corresponding to the 2nd wiring electrode of this invention is formed in the inner layer side of the circuit board as a inner layer electrode 1301. The inner layer electrode 1301 is connected with the 3rd and 4th electrode pad 111,112 through beer 1302. In addition, the terminal electrodes 1303a and 1303b are electrically connected with the surface electrode 114,115 on the circuit board. Moreover, as a latter example, when drawing 13 is substituted for and explained,

the configuration formed as a surface electrode not on a piezo-electric substrate but on the circuit board is sufficient as the 1st [corresponding to the 1st wiring electrode means of this invention shown in drawing 13], and 2nd wiring electrode 107,109, for example. Or although the 1st wiring electrode means of this invention and the 2nd wiring electrode means show the case where it is in the relation between a surface electrode and a inner layer electrode, with the above-mentioned configuration which substituted for and explained drawing 13 Mutually, a reverse configuration, i.e., the 1st wiring electrode means of this invention, may be constituted as a inner layer electrode of the circuit board, and the 2nd wiring electrode means of this invention may be constituted for the relation of these both sides as a surface electrode of the circuit board.

[0115] In addition, drawing 14 is drawing which expressed the example of a configuration of drawing 13 typically. In this drawing, the piezo-electric substrate 101 and the circuit board 113 are expressed transparent as a transparent thing for convenience. Moreover, the slash section in drawing sketches the arrangement location of the surface acoustic wave filter polar zone.

[0116] Drawing 5 (a) is used with the gestalt of the above-mentioned implementation. Moreover, the 3rd electrode pad 505 It connects with one electrode finger 403a of the 2nd IDT electrode 403. And the 4th electrode pad 506 is connected to electrode finger 404b of another side of the 3rd IDT electrode 404, and the case where electrode finger 404b of the another side saw from electrode finger 403a of the method of top Norikazu, and was moreover prepared in the reverse side was explained.

[0117] As shown not only in this but in drawing 15 (a), however, end 1501a of the 2nd wiring electrode means 3011 of this invention It connects with one electrode finger 103a of the 2nd IDT electrode 103. And you may be the surface acoustic wave filter element which other end 1501b of said 2nd wiring electrode means 3011 is connected to electrode finger 104b of another side of the 3rd IDT electrode 104, and electrode finger 104b of the another side sees from electrode finger 103a of the method of top Norikazu, and is prepared in the reverse side.

[0118] Even in this case, the same effectiveness as the gestalt of the above-mentioned implementation is demonstrated. Drawing 15 (a) is the mimetic diagram showing the configuration of the modification of the surface acoustic wave filter element of the gestalt of 1 operation of this invention shown in drawing 3 (a). Moreover, drawing 15 (b) is the surface Fig. of the circuit board corresponding to the modification shown in drawing 15 (a).

[0119] Moreover, in the above-mentioned operation gestalt, although explained focusing on the configuration which has a piezo-electric substrate and the circuit board, the surface acoustic wave filter may consist of for example, not only this but a piezo-electric substrate, and a package. As shown in drawing 16 and drawing 17 in this case, you may be the configuration in which the lower part of ceramic packages 1601 and 1701 serves as the circuit boards 1602 and 1702. In drawing 16 , signs 1603 and 1604 show an external terminal. With the configuration of drawing 17 , it differs from drawing 16 in that the inner layer electrode 116 and the external terminal (base electrode) 1704 are electrically connected with beer 1703.

[0120] Here, drawing 16 and drawing 17 are the mimetic diagrams expressed transparent like drawing 14 for explaining the example which constituted the surface acoustic wave filter from a piezo-electric substrate and a package. The slash section in drawing sketches the arrangement location of the surface acoustic wave filter polar zone.

[0121] moreover, with the gestalt of the above-mentioned implementation, the 1st wiring electrode means of this invention and the 2nd wiring electrode means of this invention as an example of the surface acoustic wave filter element arranged on a mutually different flat surface, and a surface acoustic wave filter As an example of a flat surface different the account of a top, when a piezo-electric substrate and the circuit board were used (for example, drawing 1 , drawing 3 , drawing 5 , drawing 15), the case where the surface side and inner layer side of the circuit board were used etc. was described.

[0122] As shown not only in this but in drawing 18 and drawing 19 , however, the

inside of the 1st of this invention, and the 2nd wiring electrode, One wiring electrode (107,109 of drawing 18 (a) - drawing 19 (c)) is prepared on the principal plane of a piezo-electric substrate (113 of drawing 18 (b)). The wiring electrode (1901 of drawing 19 (c)) of another side demonstrates the same effectiveness as the above also by the surface acoustic wave filter element prepared on the protective coat (1902 of drawing 19 (c)) formed on the principal plane of a piezo-electric substrate.

[0123] In addition, as shown in drawing 19 (b) and drawing 19 (c), the wiring electrode 1901 is electrically connected with electrodes 1903 and 1904 through beer 1905. Moreover, the electrode pad 108 is electrically connected with the wiring electrode 107 through beer 1906.

[0124] Especially, about this protective coat, the passivation effectiveness of an IDT electrode and the effectiveness of improving the temperature characteristic to coincidence are also acquired by using dielectric thin films, such as silicon oxide and silicon nitride.

[0125] Moreover, as long as it does not restrict connection of an electrode pad to beer and it can perform electrical installation, what kind of configuration may be used for it.

[0126] Moreover, the effectiveness is so large that the effective specific inductive capacity of a piezo-electric substrate is large in the operation gestalten 1 and 2 of this invention, and sufficient effectiveness will be acquired if effective specific inductive capacity, such as LiTaO3 and LiNbO3, is 40 or more piezo-electric substrates.

[0127] Moreover, although explained using the longitudinal-mode mold filter of three electrodes in the operation gestalten 1 and 2 of this invention, if it is the configuration that association of an input side and an output side becomes small like the operation gestalt of this invention even if this is the longitudinal-mode mold filter of two electrodes, four electrodes, and five electrodes, the same effectiveness will be acquired about a balance property. Moreover, if it is the configuration that association of an input side and an output side becomes small

similarly even if it is the filter configuration of the ladder mold not only using the longitudinal-mode mold surface acoustic wave filter of many electrodes but a surface acoustic wave resonator, or a symmetry skeleton pattern, the same effectiveness will be acquired about a balance property.

[0128] Moreover, although this operation gestalt explained one step of surface acoustic wave filter element, this may be the configuration which carried out cascade connection of two or more surface acoustic wave filter elements to multistage.

[0129] In addition, since wiring on a piezo-electric substrate becomes complicated and a wiring inter-electrode parasitism component also becomes large, it can be expected that the effectiveness of the balance property improvement by this invention is large, so that the number of an IDT electrode increases.

[0130] Moreover, although the surface acoustic wave filter element of balanced - unbalance mold and the surface acoustic wave filter of balanced - unbalance mold were explained in these operation gestalten 1 and 2, if it is the configuration that association of an input side and an output side becomes small similarly even if it is the surface acoustic wave filter element of balanced - balanced type etc., the same effectiveness will be acquired about a balance property.

[0131] Moreover, although an input side is used as an unbalance mold and the output side is used as the balanced type in these operation gestalten 1 and 2, effectiveness is the same even if this is reverse.

[0132] Moreover, as shown in drawing 20 (a) and drawing 20 (b), by mounting and carrying out the modularization of the surface acoustic wave filter element 2002 and semiconductor IC 2003 of this invention on the mounting substrate 2001, the whole equipment is made into a compact and sensibility degradation by degradation of a balance property can be suppressed. In this drawing, signs 2004 and 2005 show an external terminal and a sign 2006 is the matching circuit section. Drawing 20 (a) is a modular top view, and drawing 20 (b) is the mimetic diagram expressed transparent like drawing 14 for explaining the example of a

configuration. The slash section in drawing sketches the arrangement location of the surface acoustic wave filter polar zone.

[0133] Moreover, in the above-mentioned module, the configuration which is a low noise amplifier is sufficient as a semiconductor device. Moreover, the configuration which is a mixer is sufficient as the above-mentioned semiconductor device. Moreover, although the semi-conductor was explained as a balanced type, this may unite an unbalance-balanced type SAW filter with the device of an unbalance-unbalance mold like a GaAs switch or the switch which used the PIN diode.

[0134] Moreover, it is applicable to the communication equipment which has a balanced type RF circuit as shows the surface acoustic wave filter element or surface acoustic wave filter of this invention to drawing 21 . Thereby, sensibility degradation by degradation of the balance property of the filter for transmission or reception can be suppressed, and highly efficient mobile communication equipment can be realized.

[0135] Below, the configuration and actuation of communication equipment which have the above-mentioned balanced type RF circuit are explained, referring to drawing 21 . Here, drawing 21 is the block diagram of the balanced type high frequency circuit 2701 which used the balanced type device of this invention.

[0136] In drawing 21 , the sending signal outputted from a sending circuit 2711 is transmitted from an antenna 2705 through the transmitting amplifier 2702, the transmitting filter 2703, and a switch 2704.

[0137] Moreover, the input signal received from the antenna 2705 is inputted into a receiving circuit 2712 through a switch 2704, the receiving filter 2706, and a head amplifier 2707.

[0138] Here, since the transmitting amplifier 2702 is a balanced type and a switch 2704 is an unbalance mold, the transmitting filter 2703 serves as the configuration of having an unbalance-balance blocking output terminal. Moreover, since a head amplifier 2707 is a balanced type and a switch 2704 is an unbalance mold, the receiving filter 2706 serves as the configuration of having an

unbalance-balance blocking output terminal.

[0139] Degradation of the modulation precision at the time of transmission by degradation of a balance property can be suppressed by applying the surface acoustic wave filter of this invention to the transmitting filter 2703 and/or the receiving filter 2706. Moreover, sensibility degradation at the time of reception by degradation of a balance property can be suppressed, and a highly efficient balanced type RF circuit can be realized.

[0140] Moreover, it does not matter as the configuration of module which mentioned above the transmitting filter 2703, the transmitting amplifier 2702, or the receiving filter 2706 and a head amplifier 2707.

[0141] Moreover, it is good also as the configuration of module which mentioned above the switching device, the receiving filter, or a switching device and a transmitting filter.

[0142]

[Effect of the Invention] This invention has the advantage in which a balance property is good so that clearly from having stated above.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] (a): The mimetic diagram of the configuration of the surface acoustic wave filter element in the gestalt 1 of operation of this invention

(b): The surface Fig. of the circuit board in the gestalt 1 of operation of this invention

[Drawing 2] The side elevation showing typically the arrangement relation of the wiring electrode in the gestalt 1 of operation of this invention, and the wiring-on the circuit board electrode on the circuit board

[Drawing 3] (a): The mimetic diagram showing the configuration of other surface acoustic wave filter elements in the gestalt 1 of operation of this invention

(b): The surface Fig. of other circuit boards in the gestalt 1 of operation of this invention

[Drawing 4] The mimetic diagram showing the configuration of the surface acoustic wave filter in the gestalt 2 of operation of this invention

[Drawing 5] (a): The mimetic diagram showing the configuration of the surface acoustic wave filter element in the gestalt 2 of operation of this invention

(b): The surface Fig. of the circuit board in the gestalt 2 of operation of this invention

[Drawing 6] The side elevation showing typically the arrangement relation of the IDT electrode in the gestalt 2 of operation of this invention, and the wiring-on the circuit board electrode on the circuit board

[Drawing 7] The block diagram having shown the conventional surface acoustic wave filter typically

[Drawing 8] (a): The structure illustration of the conventional surface acoustic wave filter element

(b): The surface Fig. of the conventional circuit board

[Drawing 9] The sectional view in A-A' in drawing 8 (a)

[Drawing 10] The mimetic diagram of the configuration of the surface acoustic wave filter at the time of taking a parasitism component into consideration

[Drawing 11] (a): Drawing showing the amplitude of a surface acoustic wave filter

(b): Drawing showing a phase balance property

[Drawing 12] The decomposition perspective view of the surface acoustic wave filter of the gestalt 1 of operation of this invention

[Drawing 13] The decomposition perspective view of the surface acoustic wave filter as a modification of the gestalt of operation of this invention

[Drawing 14] Drawing which expressed the example of a configuration of drawing 13 typically

[Drawing 15] (a): The mimetic diagram showing the configuration of the modification of the surface acoustic wave filter element of the gestalt of 1 operation of this invention shown in drawing 3 (a)

(b): The surface Fig. of the circuit board corresponding to the modification shown in drawing 15 (a)

[Drawing 16] The mimetic diagram showing the package type configuration as other examples of the surface acoustic wave filter of this invention

[Drawing 17] The mimetic diagram showing other configurations of the package type surface acoustic wave filter of this invention

[Drawing 18] (a): The mimetic diagram of other examples of the surface acoustic wave filter element of this invention

(b): The surface Fig. of the circuit board corresponding to the surface acoustic wave filter element of drawing 18 (a)

[Drawing 19] (a): The mimetic diagram of other examples of the surface acoustic wave filter element of this invention

(b): The A-A' sectional view of the surface acoustic wave filter element of drawing 19 (a)

(c): The B-B' sectional view of the surface acoustic wave filter element of drawing 19 (a)

[Drawing 20] (a): The mimetic diagram showing the example of 1 configuration of the module of this invention

(b): The mimetic diagram which looked at drawing 20 (a) from the side face

[Drawing 21] The block diagram explaining the example of application to the

communication equipment of the surface acoustic wave filter of this invention

[Description of Notations]

101 Piezo-electric Substrate

102 1st IDT Electrode

103 2nd IDT Electrode

104 3rd IDT Electrode

105 1st Reflector Electrode

106 2nd Reflector Electrode

107 1st Wiring Electrode

108 1st Electrode Pad

109 2nd Wiring Electrode

110 2nd Electrode Pad

111 3rd Electrode Pad

112 4th Electrode Pad

113 Circuit Board

114 1st Wiring-on Circuit Board Electrode

115 2nd Wiring-on Circuit Board Electrode

116 3rd Wiring-on Circuit Board Electrode

301 Wiring Electrode

302 Electrode Pad

303 1st Wiring-on Circuit Board Electrode

304 2nd Wiring-on Circuit Board Electrode

305 3rd Wiring-on Circuit Board Electrode

401 Piezo-electric Substrate

402 1st IDT Electrode

403 2nd IDT Electrode

404 3rd IDT Electrode

405 1st Reflector Electrode

406 2nd Reflector Electrode

407 One Side of Balanced Type Terminal

408 Another Side of Balanced Type Terminal

409 Unbalance Mold Terminal

410 Surface Acoustic Wave Resonator

501 1st Wiring Electrode

502 1st Electrode Pad

503 2nd Wiring Electrode

504 2nd Electrode Pad

505 3rd Electrode Pad

506 4th Electrode Pad

507 5th Electrode Pad

508 6th Electrode Pad

509 Circuit Board

510 1st Wiring-on Circuit Board Electrode

511 2nd Wiring-on Circuit Board Electrode

512 3rd Wiring-on Circuit Board Electrode

513 4th Wiring-on Circuit Board Electrode

601 IDT Electrode

602 Wiring Electrode on Circuit Board

603 Wiring Electrode on Circuit Board

604 Parasitism Component

701 Piezo-electric Substrate

702 1st IDT Electrode

703 2nd IDT Electrode

704 3rd IDT Electrode

705 1st Reflector Electrode

706 2nd Reflector Electrode

707 One Side of Balanced Type Terminal

708 Another Side of Balanced Type Terminal

709 Unbalance Mold Terminal

801 1st Wiring Electrode

802 1st Electrode Pad

803 2nd Wiring Electrode

804 2nd Electrode Pad

805 3rd Wiring Electrode

806 3rd Electrode Pad

807 Circuit Board

808 1st Wiring-on Circuit Board Electrode

809 2nd Wiring-on Circuit Board Electrode

810 3rd Wiring-on Circuit Board Electrode

1001 Capacity Component

[Translation done.]

* NOTICES *

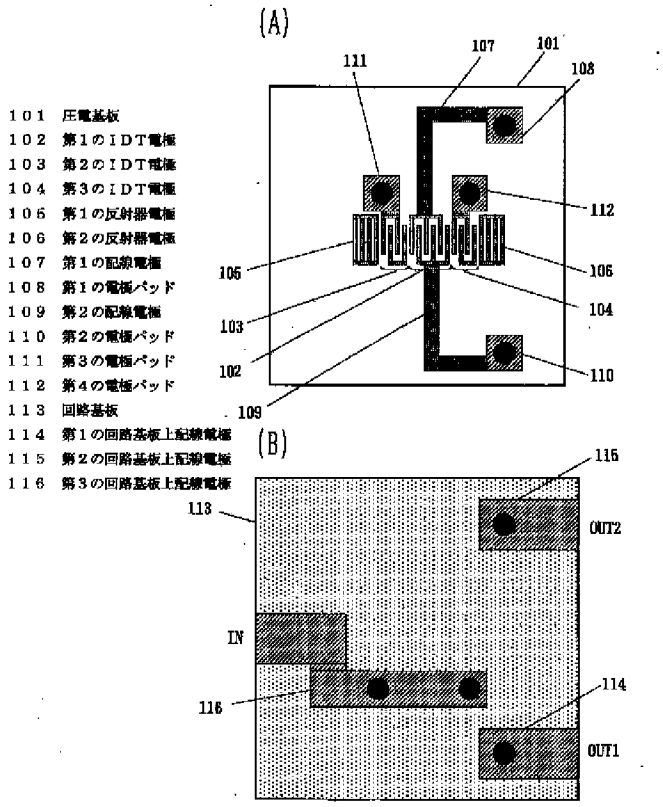
1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

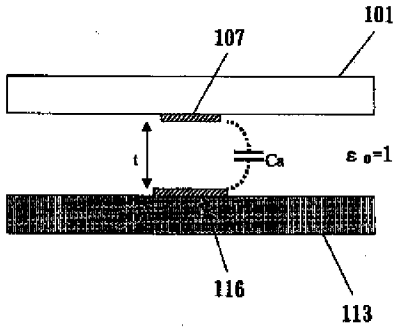
DRAWINGS

[Drawing 1]

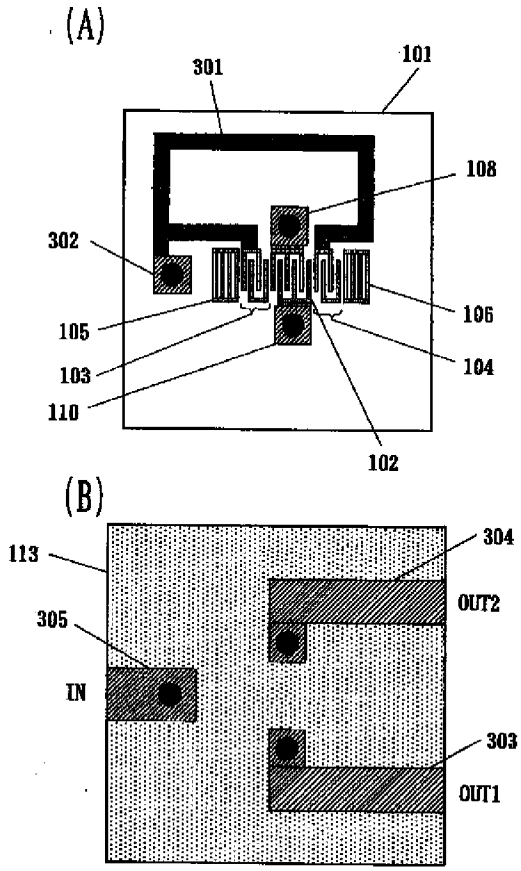


101 圧電基板
102 第１のＩＤＴ電極
103 第２のＩＤＴ電極
104 第３のＩＤＴ電極
105 第１の反射器電極
106 第２の反射器電極
107 第１の配線電極
108 第１の電極パッド
109 第２の配線電極
110 第２の電極パッド
111 第３の電極パッド
112 第４の電極パッド
113 回路基板
114 第１の回路基板上配線電極
115 第２の回路基板上配線電極
116 第３の回路基板上配線電極

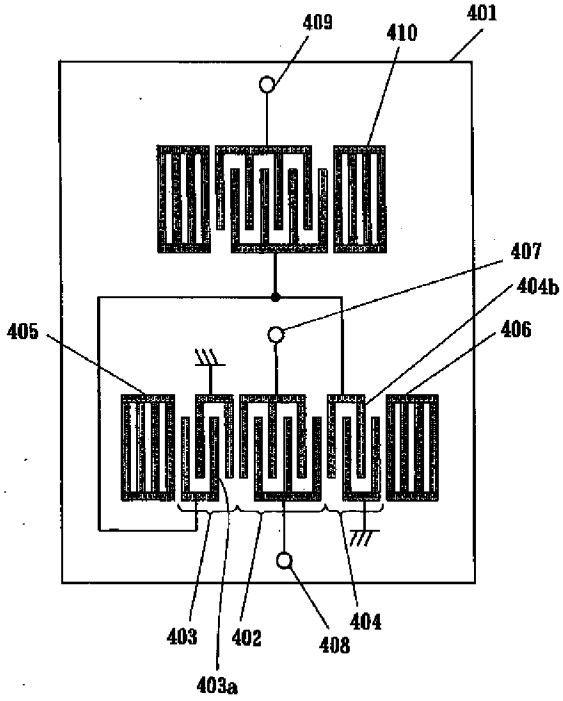
[Drawing 2]



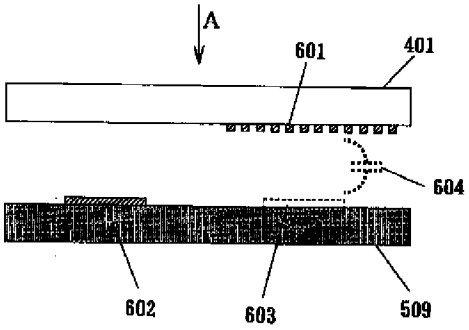
[Drawing 3]


(A)
301
101
108
302
106
105
104
103
110
102
(B)
113
304
OUT2
305
IN
303
OUT1

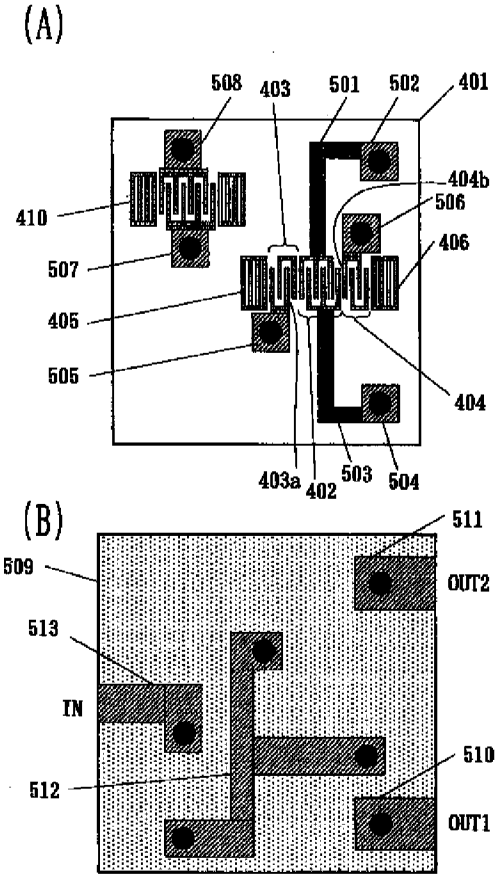
[Drawing 4]


409
410
401
407
404b
405
406
403
402
408
404
403a

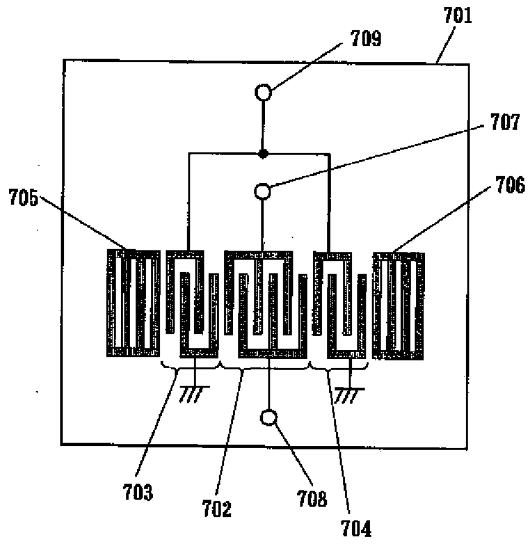
[Drawing 6]



[Drawing 5]

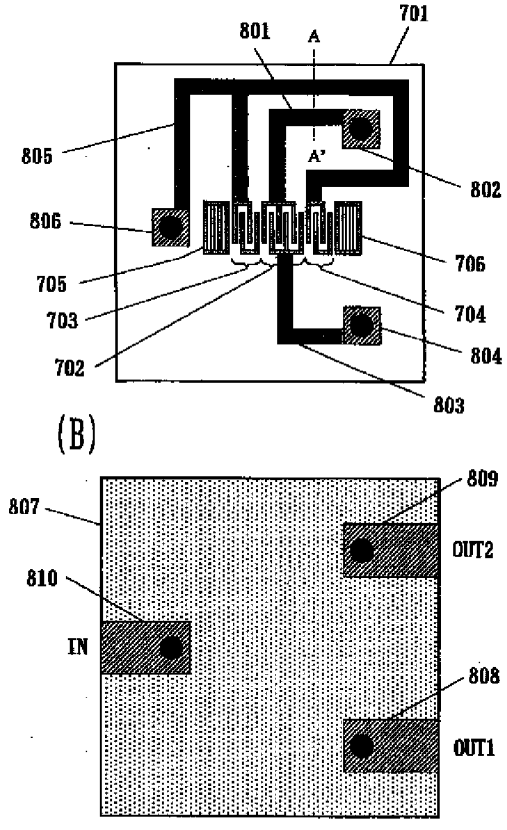


[Drawing 7]



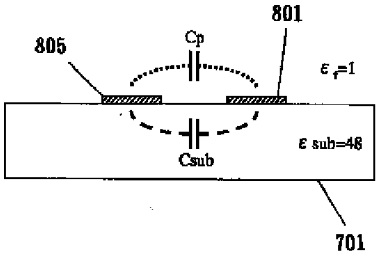
[Drawing 8]

(A)

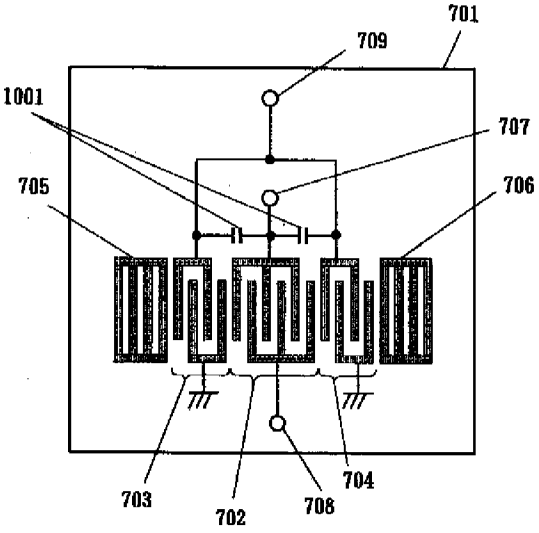


(B)

[Drawing 9]

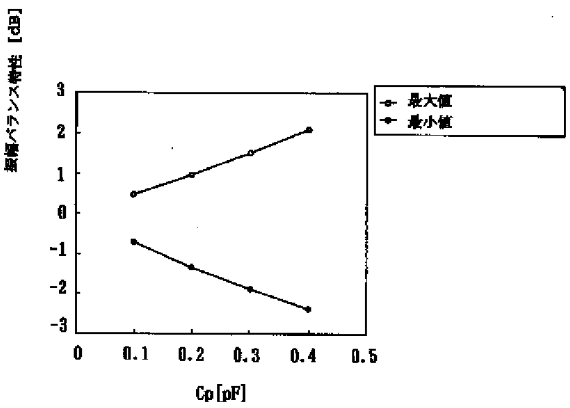


[Drawing 10]

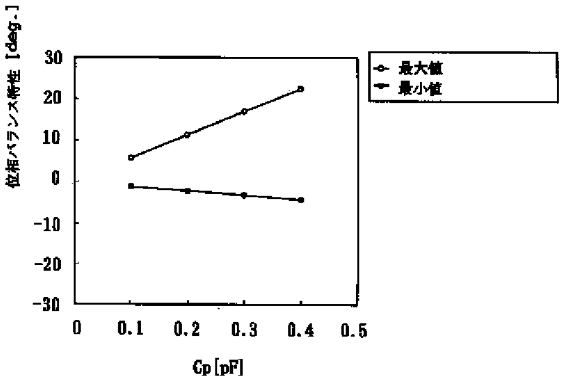


[Drawing 11]

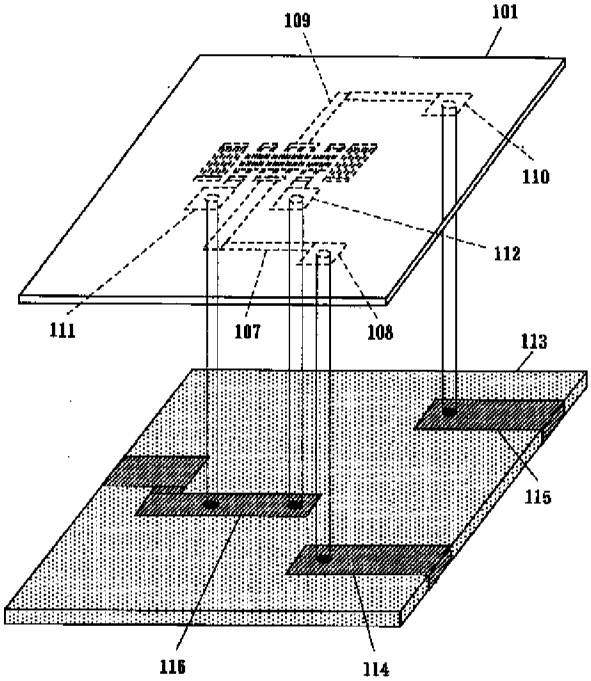
(A)



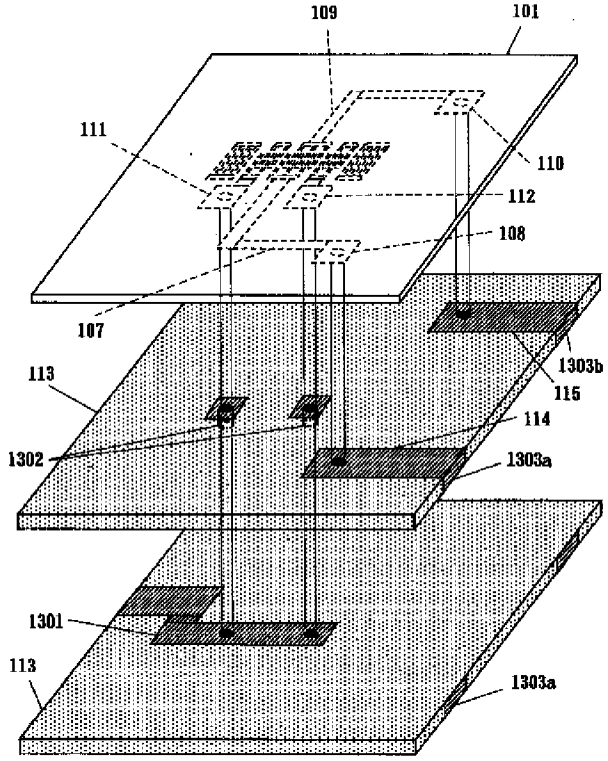
(B)



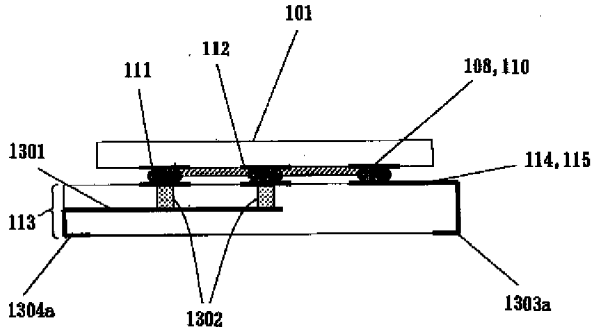
[Drawing 12]



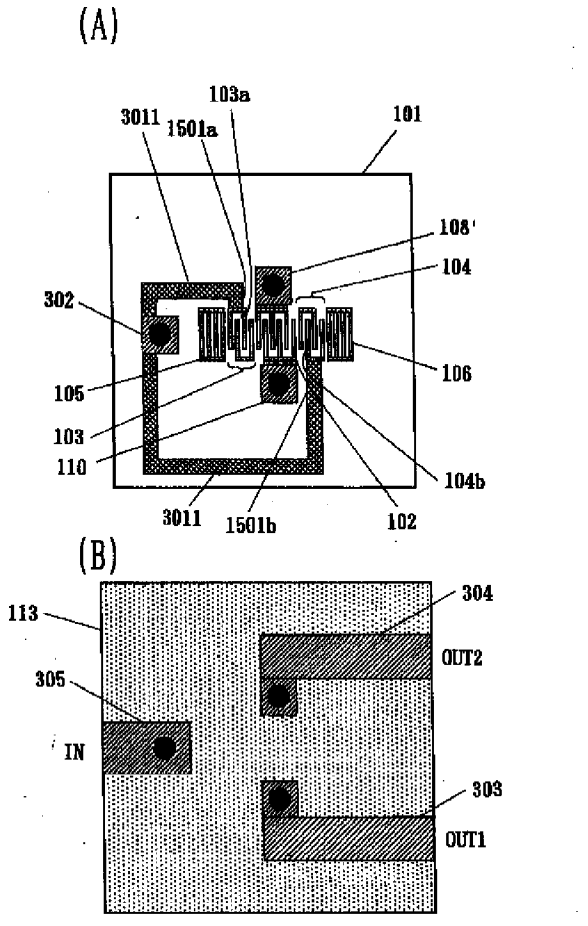
[Drawing 13]



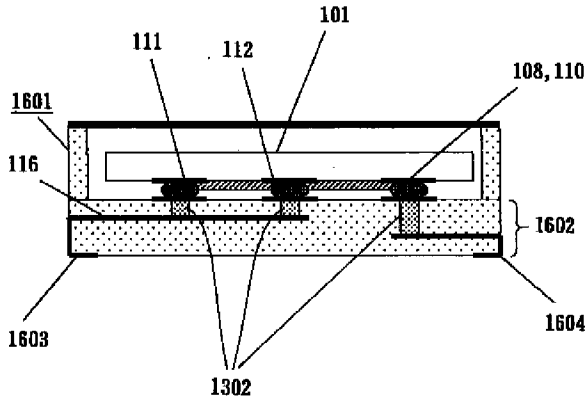
[Drawing 14]



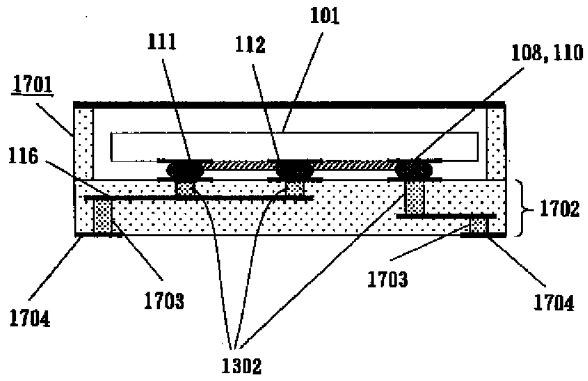
[Drawing 15]



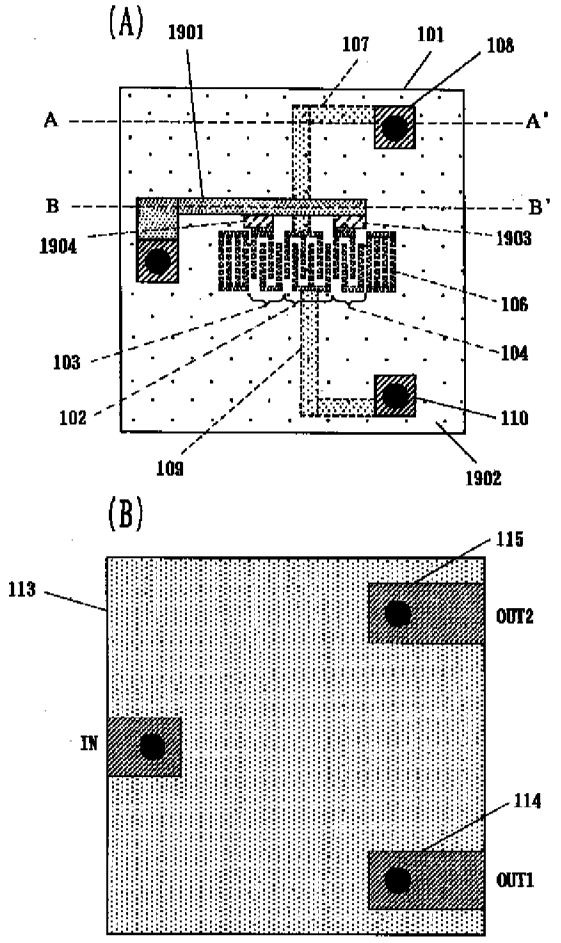
[Drawing 16]



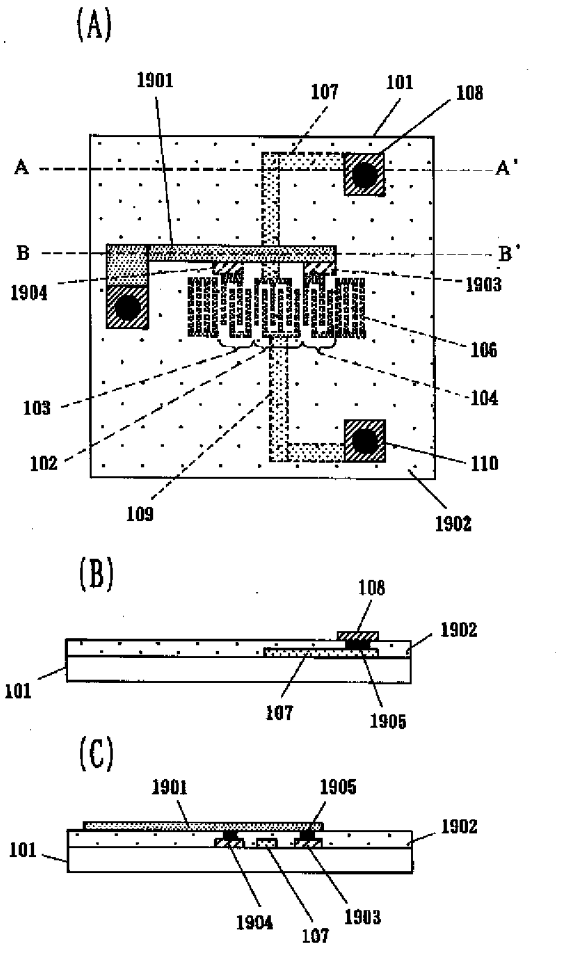
[Drawing 17]



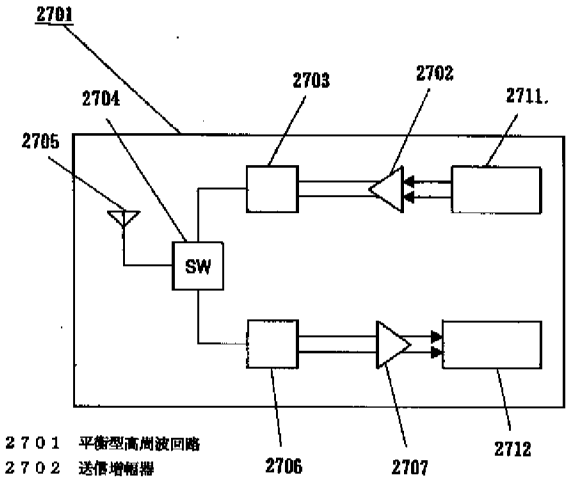
[Drawing 18]



[Drawing 19]

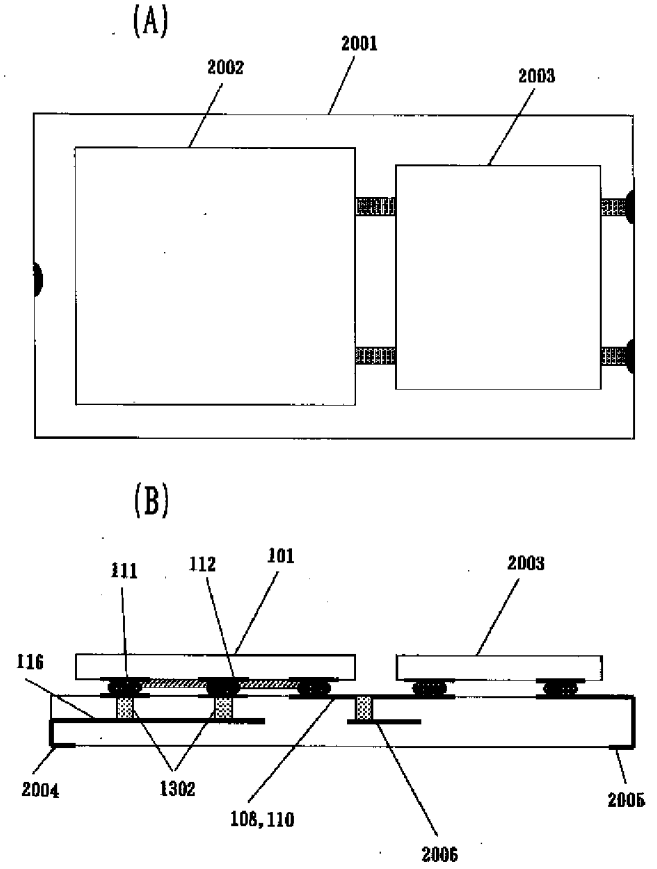


[Drawing 21]



2701 平衡型高周波回路
2702 送信増幅器
2703 送信フィルタ
2704 スイッチ
2705 アンテナ
2706 受信フィルタ
2707 受信増幅器
2711 送信回路
2712 受信回路

[Drawing 20]



[Translation done.]